Deepak Krishnankutty

🛿 (+1) 443-938-4752 | 🗷 deepakk1@umbc.edu | 🏶 deepakk0.github.io | 🖬 deepakk0 | 🎓 Deepak

Objective_

Seeking a full time position in the area of hardware and software co-design. With passionate effort, I hope to tackle the challenges in this field. I am a team member who can quickly adapt to and learn new systems, develop expertise and produce significant contributions.

Education ____

| University of Maryland Baltimore County | Maryland, USA |
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| Ph.D. candidate in Computer Engineering | Aug. 2013 - Present |
| Advisers: Dr. Chintan Patel and Dr.Ryan Robucci Research areas: Side Channel Leakage Analysis, Hardware Security, Power Analysis. | |
| National Institute of Technology, Rourkela | Orissa, India |
| Master of Technology (M.Tech.) in Computer Science & Engineering | Jun. 2007 - Jul. 2009 |
| Thesis: Implementation of a generic modular RSA on FPGA | |
| University of Calicut | Kerala, India |
| Bachelor of Technology (B.Tech.) in Computer Science & Engineering | Aug. 2002 - Aug. 2006 |
| Technical Chille | |

Technical Skills_____

| ٠ | Embedded and IoT Systems Design: | | | |
|---|---|--|--|--|
| | Hardware/Software co-design, System debugging, Sensor calibration and data acquisition, Power analysis and signal processing. | | | |
| | Languages | UML, HTML, Java, JavaScript, PHP, VHDL, Verilog, MATLAB, C, C++, Python, Assembly. | | |
| ٦ | Tools/Platforms | Rational Rose, Xilinx (ISE, EDK with MicroBlaze), ModelSim, AVR Studio, | | |
| | | Code Composer Studio (TI MSP430, Mbed ARM), PSoC Creator, MPLAB. | | |

Maryland, USA

Aug. 2013 - Present

Hardware Architecture and System Layout:

PCB design, Peripheral interfacing, Standard cell based ASIC layout design, SPICE models and simulation.

Tools/Platforms Cadence (Encounter, Virtuoso, Spectre, Capture CIS, Allegro), Autodesk Eagle, KiCad.

Research Experience

ECLIPSE Research Lab, UMBC

Research Assistant

Investigations on side channel leakage analysis of Xilinx based FPGAs and discrete TI MSP430 chips.

- Designed and developed a custom board for obtaining power analysis measurements.
- Analyzed on-board measurements using a 12-bit 4-channel ADC Via SERDES and SPI protocols.
- Analyzed off-board measurements using high speed oscilloscopes.
- Utilized GPIB protocol for oscilloscope communications.
- Utilized FTDI based serial communications for the custom board.
- Post-processing and signal analysis implemented using SVMs on MATLAB and Python.

• Optimized current board configuration for remote data collection via Python based socket protocols.

Implemented a 64-bit DES block cipher using the .180 μ m CMOS IBM PDK.

- · Comprised design RTL synthesis & custom layout.
- Implemented an SoC testbed by integrating a 128-bit AES block cipher and an open implementation of the TI MSP430.

Selected Projects

| Hardware Demonstration at Hardware Oriented Security and Trust 2016 Hardware designer and Presenter | Virginia, USA May. 2016 |
|--|----------------------------|
| Firmware Instruction Identification Using Side-Channel Analysis (3rd Position) | Mandand 11CA |
| Three-axis accelerometer data processing on FPGA Maryland, USA HARDWARE DESIGNER Aug. 2014 - Nov. 2014 • Processed three-axis acceleration data from the MPU6050 IC module and generated impulse response using a 201 tap band-pass FIR filter Implemented a 1024 FFT processor core via a Hamming window having a sample window size of 1024 samples. • Implemented custom FIFO units to stream data between FPGA and a communicating PC. | |
| Multi Functional Industrial Timer | Kerala, India |
| HARDWARE AND FIRMWARE ENGINEER A menu driven timer setup developed for managing the startup and end times of 10 external units. Implemented using a PIC18 series micro-controller. | May. 2011 - Dec. 2011 |
| Implementation of a generic modular RSA on FPGA | Orissa, India |
| Hardware Designer Implemented a high throughput 256 bit version of the RSA on a Xilinx Virtex 2 Pro. | May. 2008 - May. 2009 |

• Utilized a recursive parallel version of the Karatsuba multiplier, and a modified Extended Euclid's inversion algorithm.

Work Experience

| Mobile, Pervasive, and Sensor Systems Lab PCB Design Engineer • Designed PCBs for health kits equipped with bio-sensors. • Developed firmware for health kit boards for TI MSP430 and PSoC 6. | Maryland, USA Feb. 2020 - Present |
|---|--------------------------------------|
| University of Maryland Baltimore County | Maryland, USA |
| VISITING LECTURER Taught CMSC 313 - Introduction to Assembly And Computer Organization. Taught CMPE 310 - Systems Design and Programming. | Aug. 2018 - Dec. 2019 |
| MultiDyne | Happauge, Long Island, USA |
| ENGINEERING INTERN Successfully designed PCBs for high-speed Audio/Video transmission over fiber-optic network. Familiarization with AES and SDI standards for audio/video communications. Familiarization with CircuitWorks for PCB modelling. | May. 2018 - Aug. 2018 |
| University of Maryland Baltimore County | Maryland, USA |
| GRADUATE TEACHING ASSISTANT Assisted courses: CMPE 311 - C Programming and Embedded Systems. Provided guidance to students in various projects involving the Atmel AVR Butterfly board. CMPE 306 - Basic Circuit Theory Assisted students in getting accustomed to lab equipments. Analysis of basic RLC circuits using high speed oscilloscopes. Data capture via GPIB and post-processing of signals using MATLAB. CMPE 310 - Systems Design and Programming Guided students in the design of a minimum mode 8086 Intel microprocessor board. Familiarization with Allegro PCB Designer for board design. | Aug. 2013 - May. 2018 |
| National Institute of Technology Calicut | Kerala, India |
| Adhoc Lecturer | Dec. 2012 - May. 2013 |
| Courses Taught : Graph Theory and Combinatorics, Programming in C | |
| Jyothi Engineering College | Kerala, India |
| LECTURER Courses Taught: • Embedded Systems, Design and Analysis of Algorithms, Operating Systems. • Computer Programming in C, Computer Graphics. | Jan. 2010 - Jun. 2012 |
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Publications.

PEER-REVIEWED

Deepak Krishnankutty, Zheng Li, Ryan Robucci, Nilanjan Banerjee, Chintan Patel, "Instruction Sequence Identification and Disassembly Using Power Supply Side-Channel Analysis" in IEEE Transactions on Computers, Nov. 2020

Tracie Severson, Erick J. Rodríguez-Seda, Brien Croteau, Deepak Krishnankutty, Kiriakos Kiriakidis, Chintan Patel, Nilanjan Banerjee, Ryan Robucci, "Trust-Based Framework for Resilience to Sensor-Targeted Attacks in Cyber-Physical Systems" in 2018 IEEE American Control Conference, Jun 2018.

Brien Croteau, Deepak Krishnankutty, Kiriakos Kiriakidis, Tracie Severson, Chintan Patel, Ryan Robucci, Erick Rodriguez-Seda, Nilanjan Banerjee, "Cross-level Detection Framework for Attacks on Cyber-Physical System" in Journal of Hardware and Systems Security, Springer International Publishing, Nov 2017.

Brien Croteau, Deepak Krishnankutty, Ryan Robucci, Chintan Patel, Nilanjan Banerjee, Kiriakos Kiriakidis, Tracie Severson, Erick Rodriguez-Seda, "Cross-level detection of sensor-based deception attacks on cyber-physical system" in CYBER, Jul 2017.

Deepak Krishnankutty, Ryan Robucci, Nilanjan Banerjee, and Chintan Patel, "FISCAL: Firmware Identification Using Side-Channel Power Analysis" in 2017 IEEE 35th VLSI Test Symposium (VTS), April 2017

Sushmita Kadiyala Rao, Deepak Krishnankutty, Ryan Robucci, Nilanjan Banerjee, and Chintan Patel, "Post-Layout Estimation of Side-Channel Power Supply Signature" in Hardware Oriented Security and Trust (HOST), McLean, VA, USA, May 2015.

NON-PEER-REVIEWED

Brien Croteau, Deepak Krishnankutty, "Cyber-Physical Security Research at Umbc's Eclipse Lab" in ASME. Mechanical Engineering. March 2017; 139(03): S18–S23.