UMBC

# CMPE - 310

Midterm Review

# Outline

Instructions and Exam Format

Topics Overview

Topics for Exam with Samples

# Instructions and Exam Format

**Instructions**

Closed Book

Bring your ID (red card)

Calculators allowed

No mobile-phones, laptops, tablets, smart watches!

**Format (Four Parts – 50 Points)**

Part I – 10 Multiple-choice questions (10 Points – 1 point each)

Part II – 5 Short answer questions (15 Points – 3 points each)

Part III – 3 Fill-up questions (15 Points – 5 points each)
Fill-up missing code segments (Involves tracing code segment)
Fill-in-the-blanks (Address matching/ address space mapping)

Part IV – 1 Long Answer question (10 points)
Will be given a choice to select one among two questions.

# Topics Overview

| | |
|---|---|
| **Lecture 1** | Systems Overview (Characteristics and Metrics)<br>Distinguishing Processing Units |
| **Lecture 2** | Bus Architecture, Types, and Standards<br>Memory Bank Layout and I/O Space |
| **Lecture 3** | Instruction Pipeline<br>8086 Architecture<br>Internal programmer visible registers<br>Memory Segmentation |
| **Lecture 4** | 8284A – Clock Generator<br>8288 – Bus Controller<br>Bus Timing |
| **Lecture 5** | Addressing Modes<br>Instruction Set |
| **Lecture 6** | Types of Memory<br>Memory Chip Generic Pinout<br>Specifications for ROM, EPROM, DRAM, and SDRAM |
| **Lecture 7** | Memory Address Decoding<br>Memory Interfacing<br>Error Detection and Correction |
| **Lecture 8** | Interfacing Memory Banks<br>Memory Architecture<br>DRAM Memory |
| **Lecture 9** | DRAM Modes of Operation<br>SDRAM and DDR SDRAM<br>RAMBus and Flash |

# Topics (Lecture 1)

**Systems Overview (Characteristics and Metrics)**

**Distinguishing Processing Units**

**Possible question**

**Multi-choice. (1 point)**
Q. Which of the following metrics, measures the ability to modify a system after its initial release?

a. Flexibility
b. Maintainability
c. Correctness
d. Safety
e. Both Flexibility And Maintainability

**Short answer type. (3 points)**
Q. Write briefly on how micro-processors are different from micro-controllers. Provide examples that would illustrate the distinction.

# Topics (Lecture 2)

**Bus Architecture, Types, and Standards**

**Possible questions**

**Multi-choice. (1 point)**

Q. What does VESA stand for?

a. Video and Entertainment Systems Association
b. Video Electronic Standards Association
c. Video Electronics System Adapter
d. Virtual Entertainment Systems Application

Q. If Bus standards where arranged in the order of increasing clock speed, which of the following would be a true expression?

a. AGP > VESA > PCI > ISA
b. PCI > AGP > VESA > ISA
c. VESA> PCI > AGP > ISA
d. ISA > AGP > VESA > PCI

**Short answer type. (3 points)**

Q. Write briefly on the different types of systems buses.

# Topics (Lecture 2)

**Memory Bank Layout and I/O Space**

**Possible questions**

**Multi-choice. (1 point)**

Q. Which Address bit is mapped to the BLE in a two bank memory system?

a. A1
b. A0
c. A7
d. A19

Q. Back when 8086 processors were manufactured, the two bank memory system used two separate 8-bit wide chips. Which of the following statements stands true as a reason for this selection?

a. Memory latency was major factor back in the 1970s.
b. CPU was really fast back then. They could crunch 16-bit numbers during arithmetic operations in no time.
c. CPU could access memory in chunks or blocks back in the 1970s.
d. Memory modules were manufactured 8-bit wide with moderate latencies.

# Topics (Lecture 3)

**Instruction Pipeline**
**8086 Architecture**
**Internal programmer visible registers**
**Memory Segmentation**

**Possible questions**

**Multi-choice. (1 point)**
Q. Which flag(s) is/are set when a borrow occurs after subtraction?
a. Zero Flag
b. Carry Flag
c. Zero Flag and Carry Flag
d. Direction Flag

**Short answer type. (3 points)**
Q. What are the different segments registers available to a programmer? Explain each segment register's purpose briefly in one-two sentences.

# Topics (Lecture 4)

**8284A – Clock Generator**
**8288 – Bus Controller**
**Bus Timing**

**Possible questions**

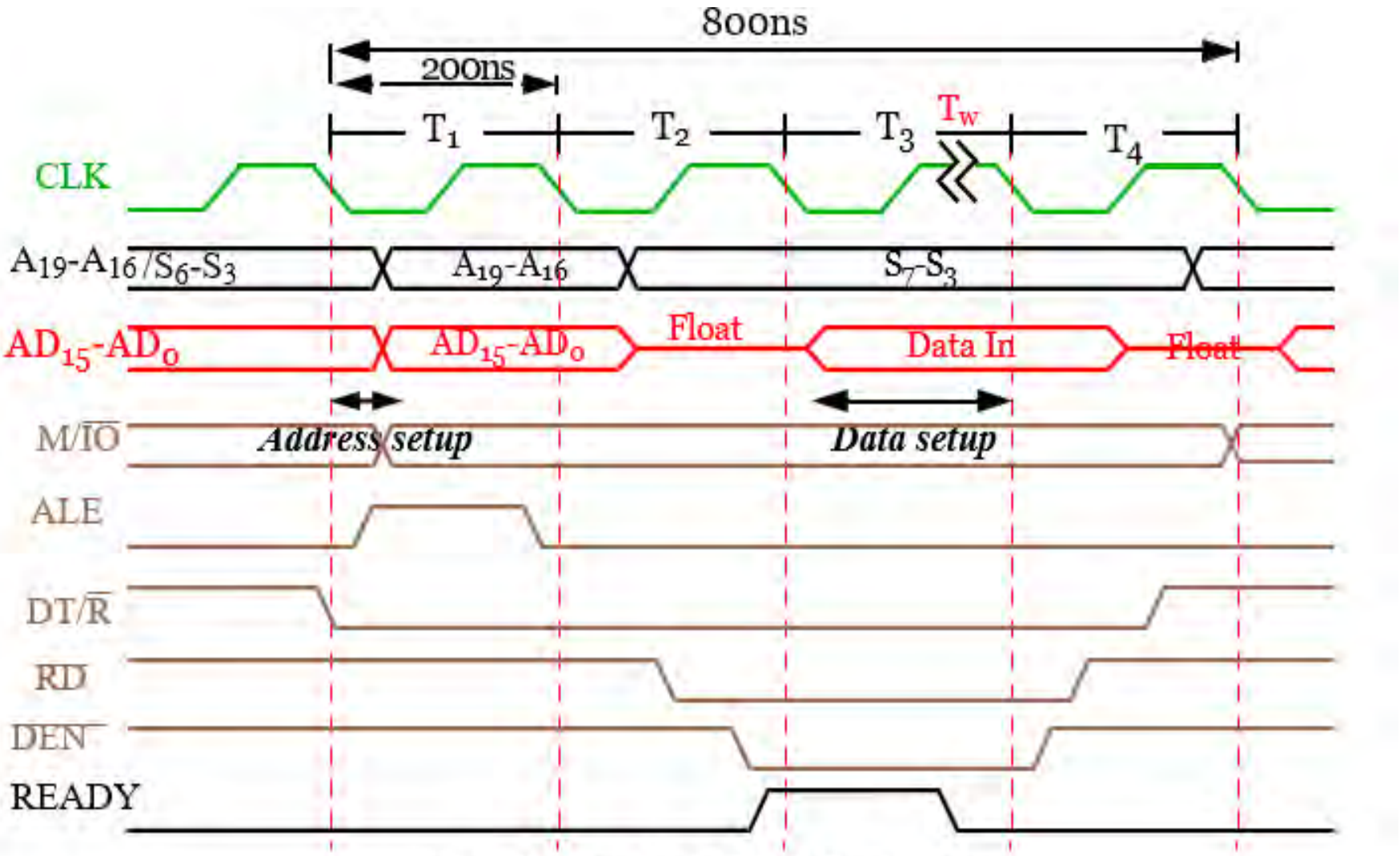
**Multi-choice. (1 point)**
Q. If a Memory/ IO device is **not** ready to transmit data, a wait state $T_w$ is introduced between which two states?
a. $T_1$ and $T_2$
b. $T_2$ and $T_3$
c. $T_4$ and $T_5$
d. $T_3$ and $T_4$

**Short Answer (3 Points)**
Q. What is the purpose of a divide-by-3 counter in 8284A (Clock Generator)?

**Long Answer (Partial – 5 Points)**

Q. Draw the BUS timing diagram for a “memory” read operation. Your timing diagram must include the states for the following pins:
CLK, A19-A16/ S6- S3, S7, AD15-AD0, ALE, M/ $\overline{IO}$ , $\overline{RD}$ , DT/ $\overline{R}$ , $\overline{DEN}$, and READY.
Explain what happens during each cycle ($T_1$-$T_4$) and optional $T_w$ .

# Topics (Lecture 4)




**Bus Timing for a Read Operation**

# Topics (Lecture 5)

**Addressing Modes**
**Instruction Set**

**Possible questions**

**Multi-choice. (1 point)**
Q. Which of the following is **not** a legal instruction for the 80x86 processor?

a. add eax, ebx
b. add [eax], [ebx]
c. sub [eax], ebx
d. sub eax, ecx

Q. Which of the following is an example for **based index addressing**?

a. add eax, [esi+34]
b. add eax, [ebx+esi+34]
c. sub eax, [ebx+34]
d. sub eax, [ebx]

**Fill-up question. (5 points)**
Q. Mystery! Based on assignments but way more simpler!

# Topics (Lecture 6)

**Types of Memory**
**Memory Chip Generic Pinout**
**Specifications for ROM, EPROM, DRAM, and SDRAM**

**Possible questions**

**Multi-choice. (1 point)**
Q. A memory device with 16 address pins and 16 data pins is specified by

a. 64 X 4
b. 16 X 4
c. 64K X 16
d. 16 X 16

**Short Answer (3 Points)**
Q. List the different types of ROM and briefly describe the characteristics of each.

# Topics (Lecture 7)

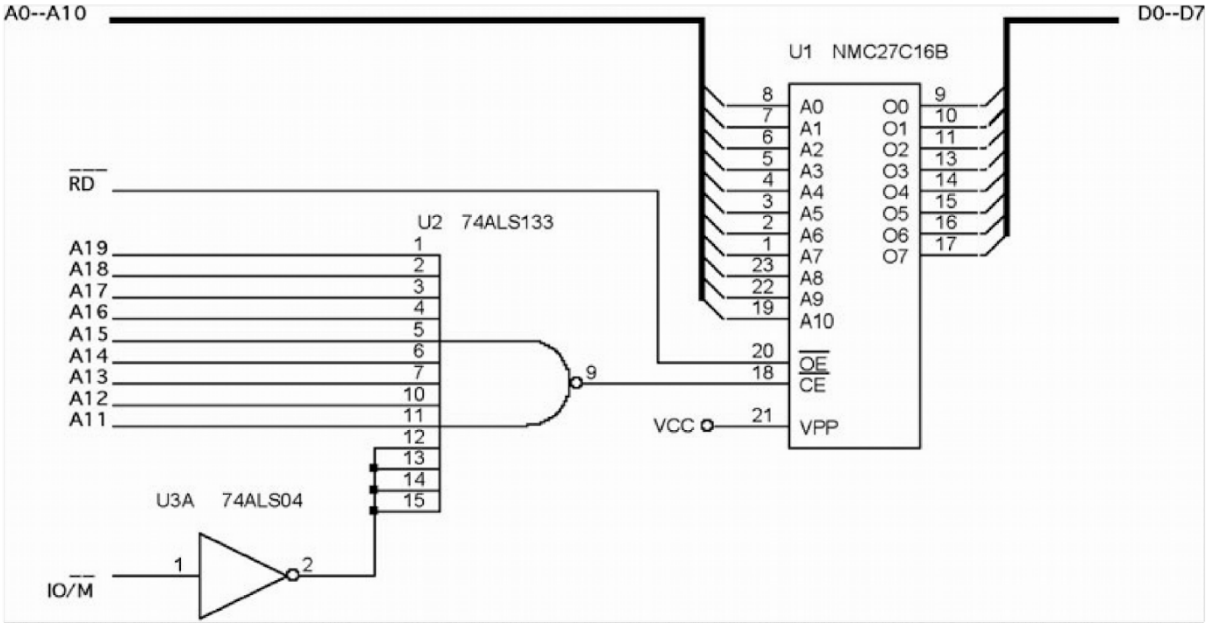
**Memory Address Decoding**
**Memory Interfacing**
**Error Detection and Correction**

# Topics (Lecture 7)

**Possible questions**

**Fill-in-the-blanks. (5 points)**

Q. The following diagram shows a common memory decoding strategy for an 8088 microprocessor interfaced with a 2716 EPROM (2K x 8).




The smallest address mapped into memory is _____. (Give you answer in hex)

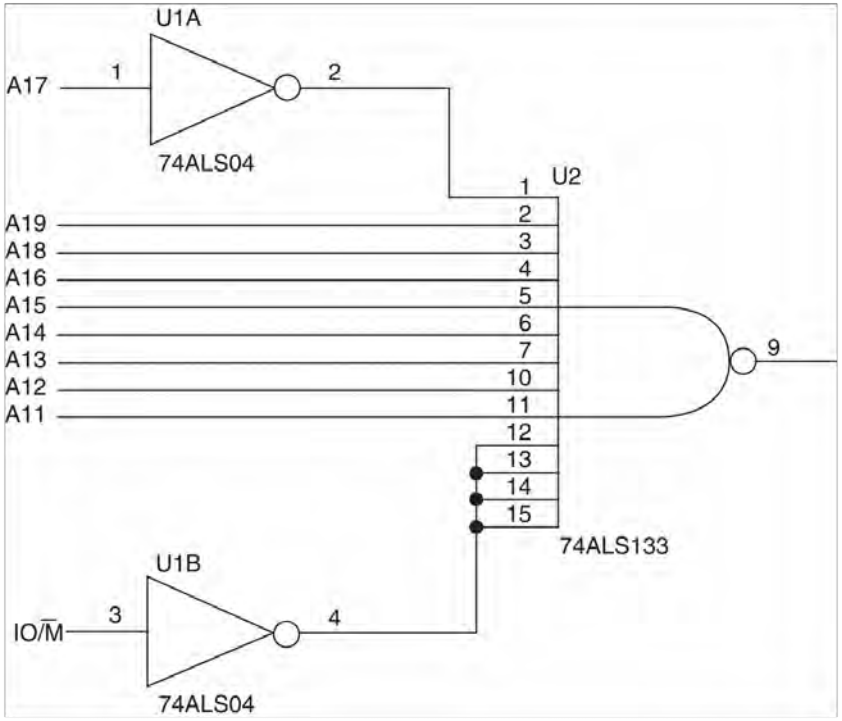
The largest address mapped into memory is _____. (Give you answer in hex)

(continued in the next slide)

# Topics (Lecture 7)

(Continued from previous slide)

If the chip enable signal is determined using the following circuit, does the address mapping change? _____ (Yes/ No)



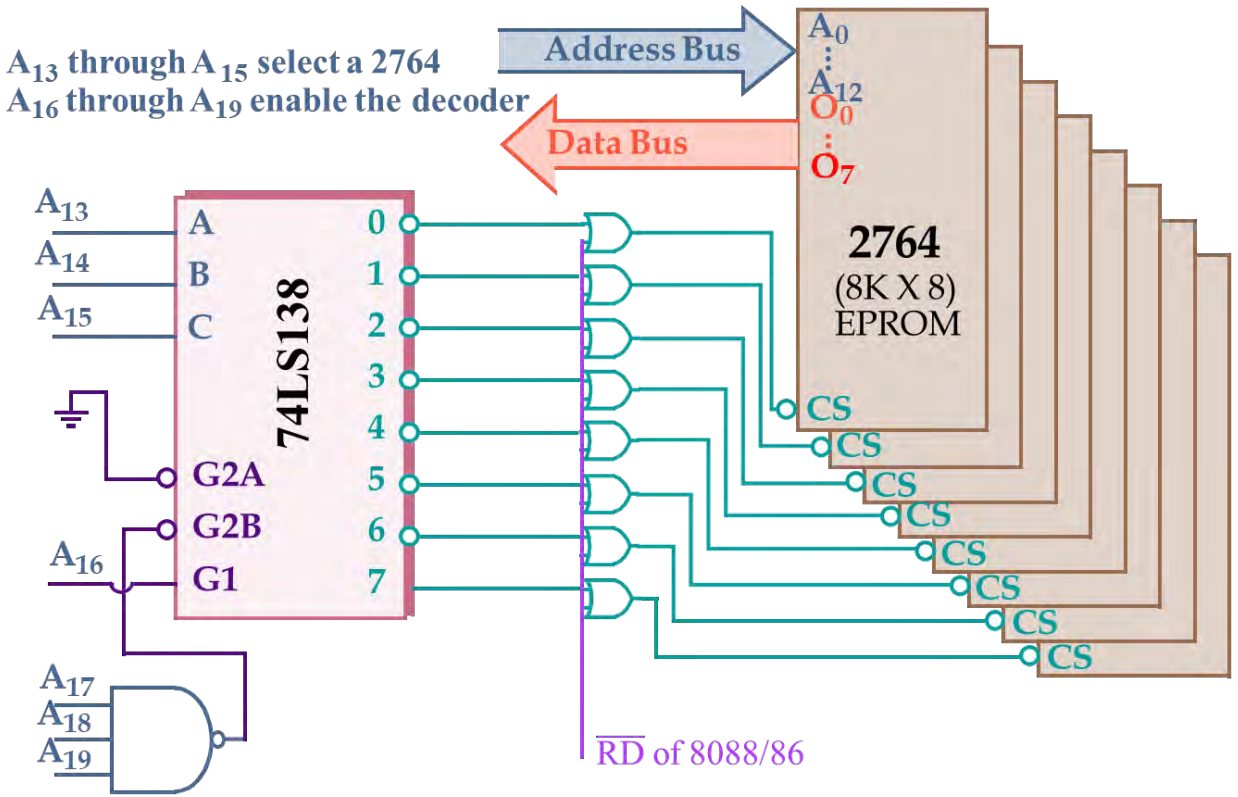

The smallest address mapped into memory is _____. (Give you answer in hex)
The largest address mapped into memory is _____. (Give you answer in hex)

# Topics (Lecture 7)

**Possible questions**

**Fill-in-the-blanks. (5 points)**

Q. The following diagram shows a common memory decoding strategy for an 8088 microprocessor interfaced with a 2764 EPROM (8K x 8).




The smallest address mapped into memory is _____. (Give you answer in hex)

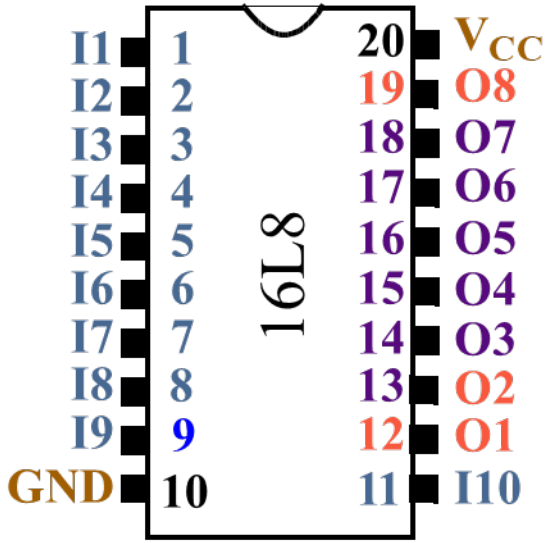
The largest address mapped into memory is _____. (Give you answer in hex)

(continued in the next slide)

# Topics (Lecture 7)

(Continued from previous slide)

Now replace the 74LS138 with a PAL 16L8 below.




```
;pins 1   2   3   4   5   6   7   8   9   10
      A19 A18 A17 A16 A15 A14 A13 NC  NC  GND
;pins 11  12  13  14  15  16  17  18  19  20
      NC  O8  O7  O6  O5  O4  O3  O2  O1  VCC
```

Represent AND using * and NOT using an overbar.

The equation for O1 is _____.

The equation for O4 is _____.

The equation for O8 is _____.

# Topics (Lecture 8)

**Interfacing Memory Banks**
**Memory Architecture**
**DRAM Memory**

**Possible questions**

**Short answer type. (3 points)**
Q. Differentiate between SRAMs and DRAMs.

**Long Answer (Partial – 5 Points)**

Q. Differentiate between RAS-only refresh and CAS-before-RAS refresh scheme in DRAMs. Illustrate with timings diagrams for each scheme showing the state of $\overline{RAS}$ , $\overline{CAS}$, and Address pins.

# Topics (Lecture 9)

**DRAM Modes of Operation**
**SDRAM and DDR SDRAM**
**RAMBus and Flash**

**Possible questions**

**Multi-choice. (1 point)**

Q. Which of the following is **true** about Flash devices?

a. Flash File devices benefit from asymmetric block sizes during in-system programming
b. Parameter blocks in Boot Block devices store system configurations tables.
c. Individual blocks in a Bulk Erase Flash devices can be erased independently.
d. Parameter blocks within Boot Block devices are larger than main blocks.

**Short answer type. (3 points)**

Q. Assume that a 1 MB DRAM device implements page mode of operation. This device is realized by a pair of two bank 256K X 8 chips. There are 4 blocks per chip. Everytime an address is specified for a read operation, page mode fetches data from 8 consecutive address locations per block. Determine the page size for this device.