UMBC

CMPE - 310

Final Exam Review

Outline

Instructions and exam format

Topics overview

Topics for exam with samples

Instructions and exam format

Instructions

Closed Book

Bring your ID (red card)

Calculators allowed

No mobile-phones, laptops, tablets, smart watches!

Format (Four Parts – 100 Points)

Part I – 10 Multiple-choice questions (10 Points – 1 point each)

Part II – 5 Short answer questions (30 Points – 6 points each)

Part III – 5 Fill-up questions (40 Points – 8 points each)
Fill-up missing code segments (Involves tracing code segment)
Fill-in-the-blanks (Address translations – paging and segmentation)

Part IV – 2 Long Answer questions (20 Points – 10 points each)
Will be given a choice to select one among two questions for each case.

Topics overview

Lecture 10	I/O Mapping, Interfacing, Port Decoding Programmable Peripheral Interface (PPI) - 8255
Lecture 11	Programmable Keyboard/Display Interface – 8279 Programmable Interval Timer - 8254
Lecture 12	Programmable Communications Interface – 16550 Serial and parallel ports ADC and DAC
Lecture 13	Interrupts – Concept, Implementation, Types Programmable Interrupt Controller – 8259
Lecture 14	Direct Memory Access Controller - 8237
Lecture 15	Storage and Display Technologies Magnetic, Optical and Solid State Devices Display Devices – TTL and Analog RGB, LCD, LED, OLED
Lecture 16	Bus Interfacing Standards – ISA, EISA, VESA, PCI, USB, AGP
Lecture 17	OS Concepts Processes and Tasks Memory Management Paging Techniques Virtual Memory TLBs – Translation Lookaside Buffers
Lecture 18	Segmentation - Descriptors and Selectors Segment Address Translation
Lecture 19	Paging and Segmentation Privilege Levels Call Gates

Topics (Lecture 10)

I/O Mapping, Interfacing, Port Decoding

Programmable Peripheral Interface (PPI) - 8255

Possible question

Multi-choice. (1 point)

Q. Which among the following statements is true?

a. Variable I/O addresses in an 8086 processor is specified using 8-bits.

b. Fixed I/O addresses in an 8086 processor is specified using 8-bits.

c. IN and OUT instructions in 8086 transfer data between I/O device and the DL, DX or EDX register.

d. IN and OUT instructions are the only way to reference memory in the Memory-mapped I/O scheme.

Short answer type. (6 points)

Q. Distinguish between Isolated and Memory-Mapped I/O. Given a system with limited main memory, which scheme would be well suited for implementation?

Topics (Lecture 11)

Programmable Keyboard/Display Interface – 8279

Programmable Interval Timer - 8254

Possible questions

Multi-choice. (1 point)

Q. Which among the following statements is true about the 8254 (Programmable Interval Timer)?

a. The 8254 comprises three independent 8-bit counters.
b. 8254 can be used to refresh DRAM memory.
c. 8254's outputs can be used as a timing source (system clock) for the 8086.
d. 8254 outputs can only be triggered using software.

Short answer type. (6 points)

Q. What is the function of clock input in an 8279?

Topics (Lecture 12)

Programmable Communications Interface – 16550
Serial and parallel ports
ADC and DAC

Possible questions

Multi-choice. (1 point)

Q. Which among the following statements is true about the 16550 (Programmable Communications Interface)?

a. The number programmed into the baud-rate generator, causes 16550 to generate a clock 8 times the baud-rate.
b. 16550 transmits data via a parallel interface.
c. 16550 can have its own independent clock source.
d. There is only one shared 16 byte FIFO buffer for receiving and transmitting data.

Short answer type. (6 points)

Q. Distinguish between serial ports and parallel ports. According to you, which port technology is prone to more errors in data transmission and why?

Q. What does the term “resolution” mean in the context of a DAC? What is the purpose of an INTR pin on an ADC chip?

Topics (Lecture 13)

Interrupts – Concept, Implementation, Types

Programmable Interrupt Controller – 8259

Possible questions

Multi-choice. (1 point)

Q. Which among the following statements is true about the 8259 (Programmable Interrupt Controller)?

a. 8259 can service up to 32 interrupt requests in the master/slave configuration.

b. With rotating priority configured, once an interrupt request is processed, it is assigned the lowest priority value.

c. 8259 cannot be configured to turn off any of its input interrupt request lines.

d. The INTA pin on 8259 is used to acknowledge interrupt requests from other I/O peripherals/devices in the system and it is interfaced directly to specific input pins on other I/O devices.

Short answer type. (6 points)

Q. Distinguish between hardware and software interrupts. Provide examples.

Q. List and explain the sequence of steps a microprocessor undertakes after it acknowledges an interrupt.

Topics (Lecture 14)

Direct Memory Access Controller - 8237

Possible questions

Short Answer (6 Points)
Q. Explain the need for a DMAC (Direct Memory Access Controller) in a system.

Topics (Lecture 15)

Storage and Display Technologies
Magnetic, Optical and Solid State Devices
Display Devices – TTL and Analog RGB, LCD, LED, OLED

Possible questions

Short Answer (6 Points)

Q. Briefly discuss the storage technologies – Magnetic hard disk, Optical disk, and SSD.

Topics (Lecture 16)

Bus Interfacing Standards – ISA, EISA, VESA, PCI, USB, AGP

Possible questions

Multi-choice. (1 point)

Q. Which of the following is true about PCI?

a. Requires the processor to determine the type of interfaced device through a series of handshaking and control commands.

b. PCI has its own bus independent of processor type and architecture.

c. PCI requires its configuration space to be populated by the OS during boot up.

d. PCI maintains a serial communication with its devices.

Short Answer (6 Points)

Q. Briefly explain the features of an ISA Bus. How is the EISA different from ISA?

Topics (Lecture 17)

OS Concepts

Processes and Tasks, Memory Management, Paging Techniques, Virtual Memory

TLBs – Translation Lookaside Buffers

Possible questions

Multi-choice. (1 point)

Q. Which of the following is true about external fragmentation

a. Paging causes external fragmentation.

b. Can be reduced by means of memory compaction.

c. Occurs when a process memory resource request leaves left over space within a partition.

d. Can occur only in smaller capacity memories such as Cache.

Short Answer (6 Points)

Q. Briefly explain the features of an ISA Bus. How is the EISA different from ISA?

Q. Explain the function of a TLB (Translation Lookaside Buffer).

Long Answer (Partial – 5 Points)

Q. Differentiate between fixed-sized partitions and variable-sized partitions.

Q. What are the effects of implementing Page Tables in relation to its size and performance?

Topics (Lecture 18)

Segmentation - Descriptors and Selectors
Segment Address Translation

Possible questions

Multi-choice. (1 point)
Q. Which of the following is true about external fragmentation
a. Paging causes external fragmentation.
b. Can be reduced by means of memory compaction.
c. Occurs when a process memory resource request leaves left over space within a partition.
d. Can occur only in smaller capacity memories such as Cache.

Short Answer (6 Points)
Q. What are selectors and descriptors in the context of protected memory?
Q. What is the function of a GDT? Why is there a need for two separate tables GDT and LDT?

Topics (Lecture 19)

Paging and Segmentation
Privilege Levels
Call Gates

Possible questions

Short Answer (6 Points)
Q. What is the purpose of a call gate? Explain its mechanism.
Q. What are the different types of privileged instructions? What are the different checks an OS makes when a descriptor table entry is accessed by a process?

Topics (Lecture 19)

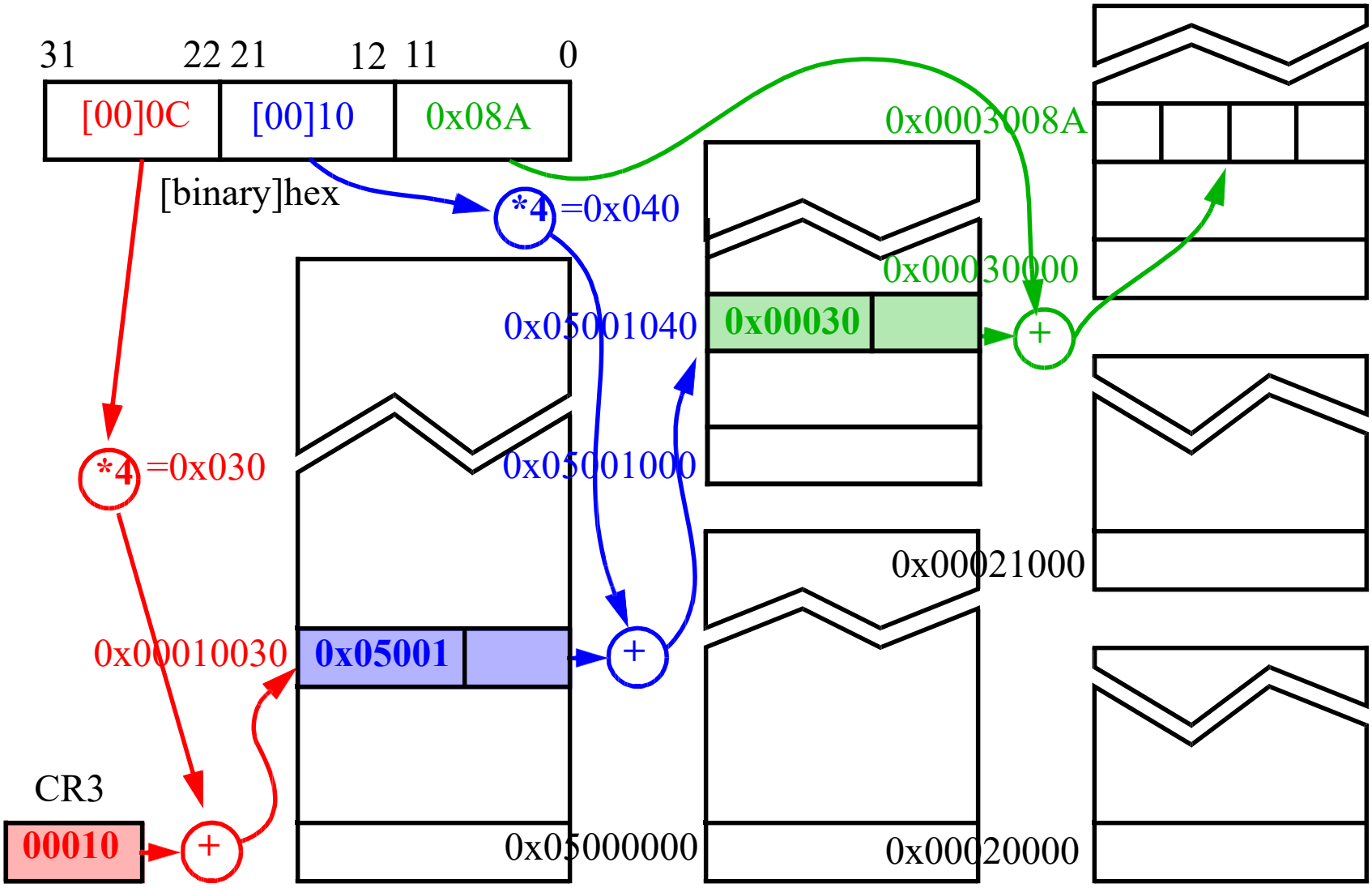
Paging and Segmentation
Privilege Levels
Call Gates

Possible questions

Fill up question (8 Points)

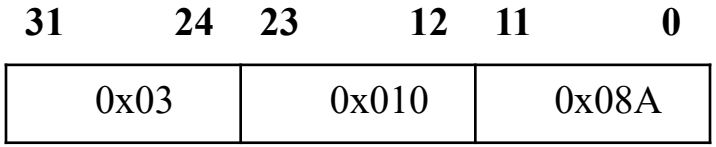
Q. An OS implements its virtual memory scheme with a page directory comprising 256 entries, and page tables comprising 4096 entries. Given the following page directory contents and page tables loaded into the memory, fill up the spaces provided with the translated information. Page frames are 16 bits wide and their offsets are byte addressable.
The virtual address to be translated is **0x0301008A**.
All the answers must be specified in hexadecimal.

Topics (Lecture 19)



Topics (Lecture 19)

Virtual Address: **0x0301008A**



Page Directory

0x0000100C

0x05001

CR3

00001

Page Table

0x05001040

0x0003008A
0x00030

0x05001000

Page Frames

Nibble	**4**	**3**	**2**	**1**
	45	36	**A1**	**C3**

0x00030000
