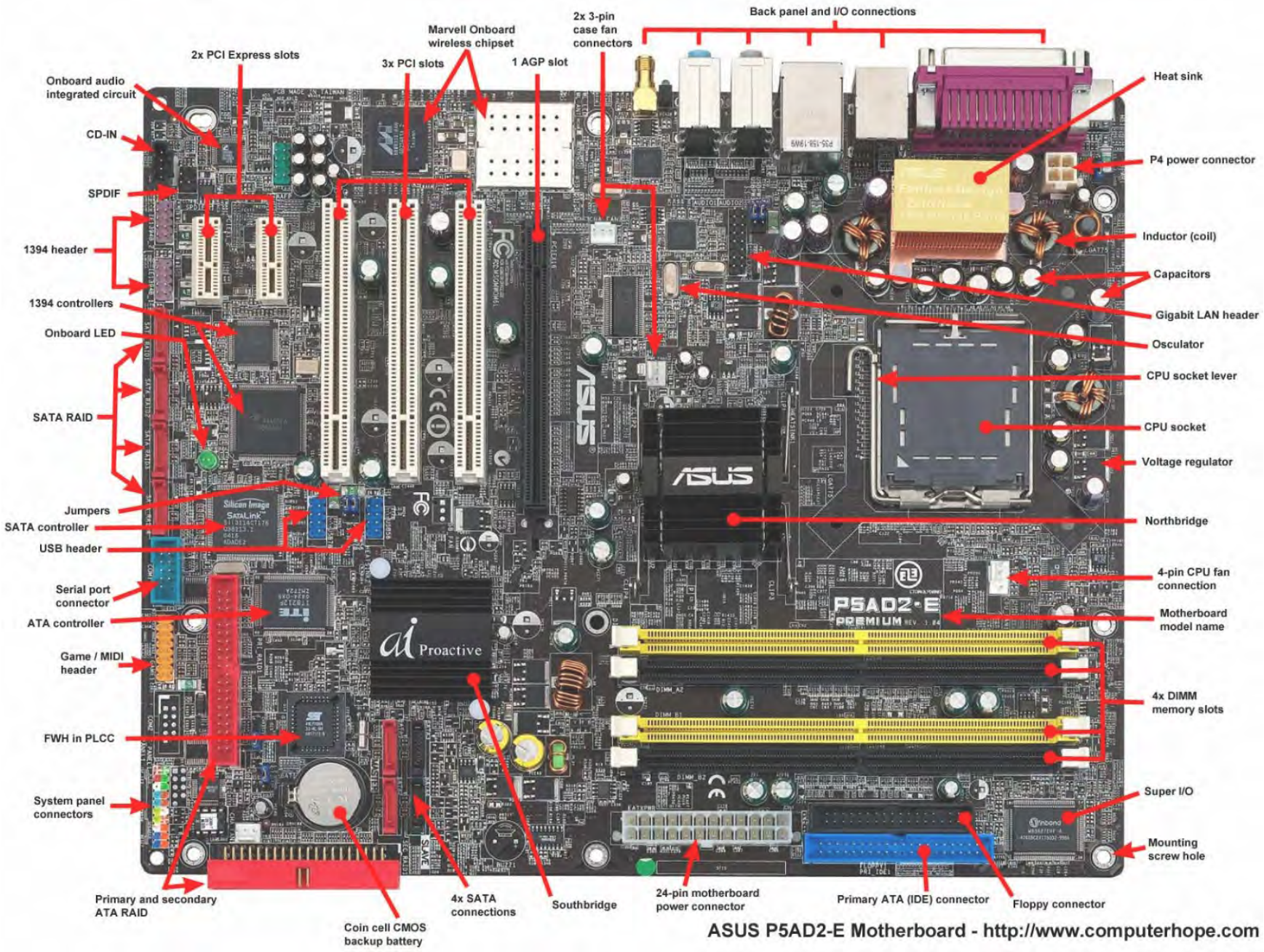
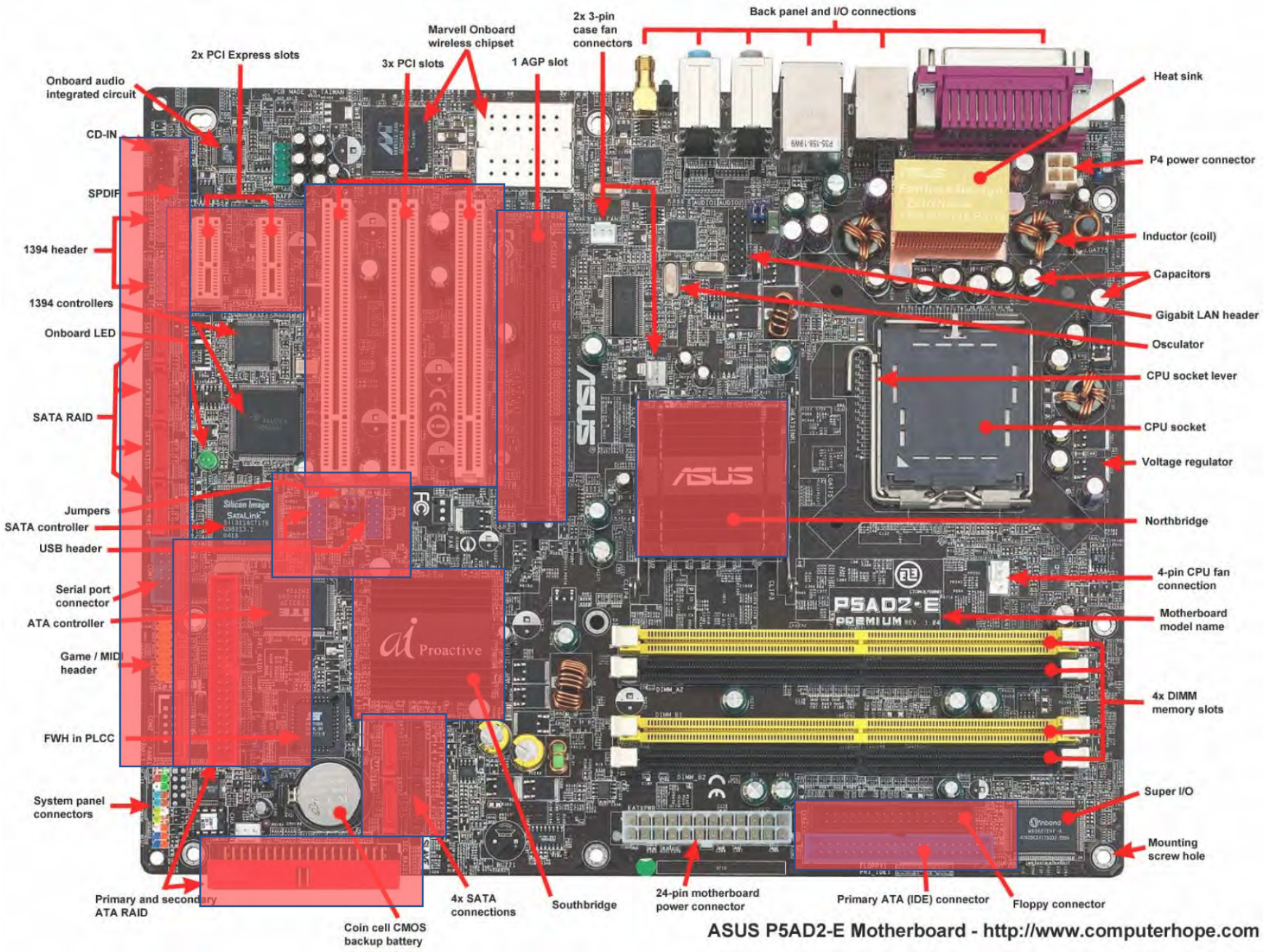
UMBC

CMPE - 310

Lecture 16 – Bus Interfacing



Source: computerhope.com, https://www.computerhope.com/cdn/bigmb.jpg



Source: computerhope.com, https://www.computerhope.com/cdn/bigmb.jpg

Bus Interfaces

Different types of buses:

- ISA (Industry Standard Architecture)
- EISA (Extended ISA)
- VESA (Video Electronics Standards Association, VL Bus)
- PCI (Peripheral Component Interconnect)
- USB (Universal Serial Bus)
- AGP (Advanced Graphics Port)

ISA is the oldest of all these and today's computers still have a ISA bus interface in form of an ISA slot (connection) on the main board.

ISA has 8-bit and 16-bit standards along with the 32-bit version (EISA).

All three versions operate at 8MHz.

8-Bit ISA Bus connector

Pin #			
1	GND	$\overline{\text{IO CHK}}$	
2	RESET		D0-D7
3	+5V		
4	IRQ2		
5	-5V		
6	DRQ2		
7	-12V		
8	OWS		
9	+12V		
10	GND	IO RDY	
11	MEMW	AEN	
12	MEMR		A0-A19
13	IOW		
14	IOR		
15	DACK3		
16	DRQ3		
17	DACK1		
18	DRQ1		
19	RESET		
20	CLOCK		
21	IRQ7		
22	IRQ6		
23	IRQ5		
24	IRQ4		
25	IRQ3		
26	DACK2		
27	T/C		
28	ALE		
29	+5V		
30	OSC		
31	GND		

ISA Bus Connector Contains

8- bit Data Bus

Demultiplexed 20-bit address Bus

I/O and Memory Control Signals

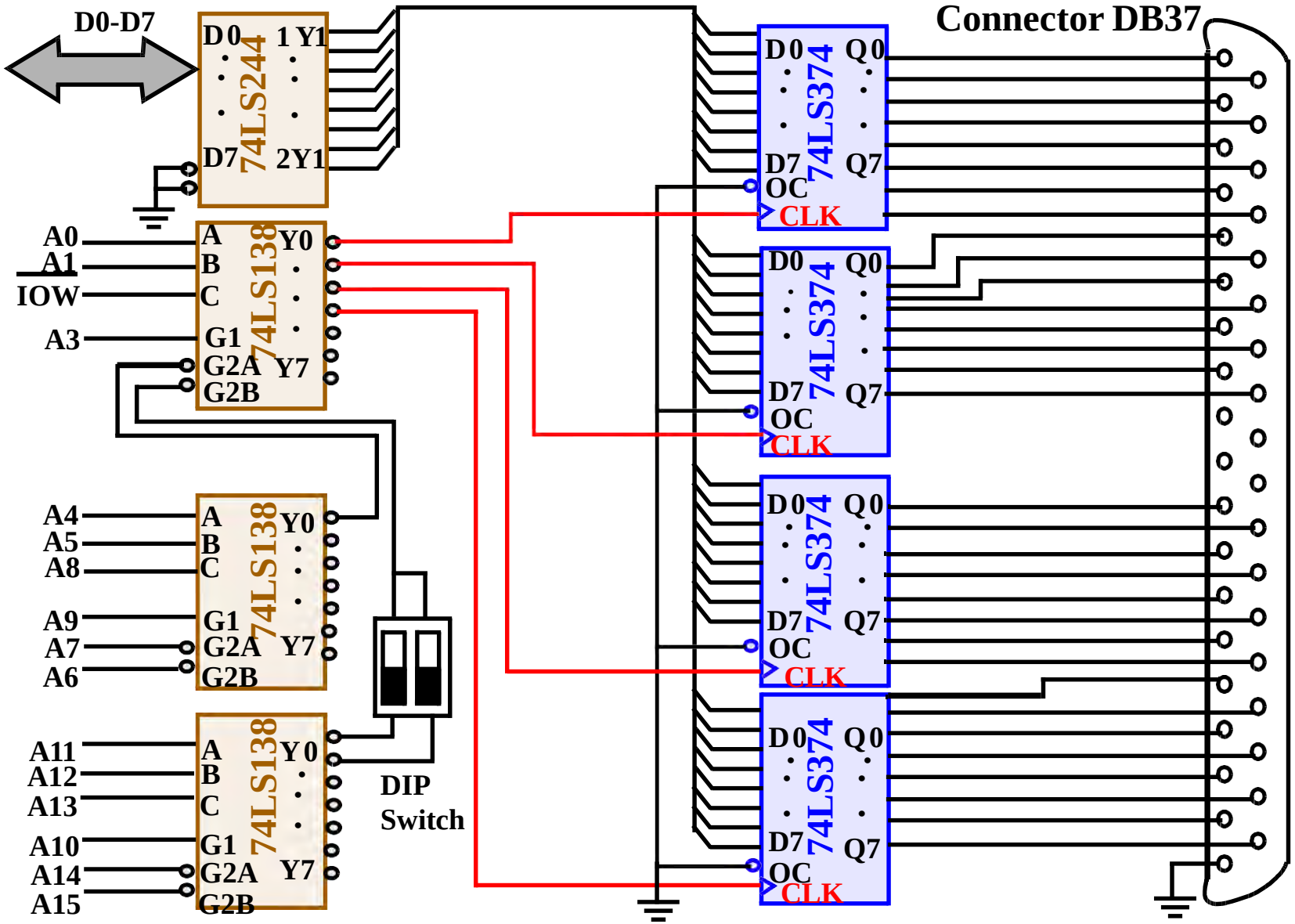
Interrupt Request Lines (IRQ2->IRQ7)

DMA channels 1-3 Control Signals

Power, RESET and misc. signals

Source: http://smallformfactors.mil-embedded.com/articles/isa-bus-going-strong-pc104/

8-Bit ISA Bus Output Interface



8-Bit ISA Bus Output Interface

4, 8-bit latches interfaced using an ISA interface for 32 bit parallel data.

74LS244 buffers used to ensure only **one** lower power TTL load on the bus.
Loading is important as many cards can be connected on the bus.

The DIP switch can be used to change the address thus avoiding address conflicts with other cards in the system.

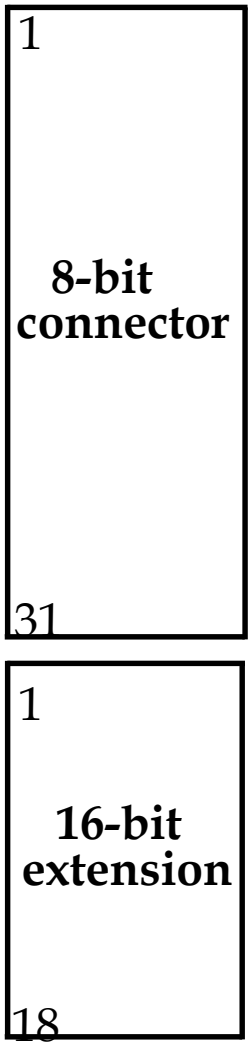
See text for examples of output interface using a PLD and also an ISA bus input interface for A-to-D converters.

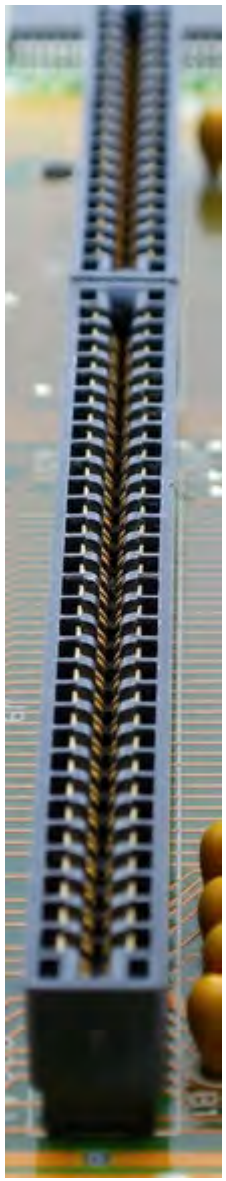
16-bit ISA bus has an additional connector attached behind the 8-bit connector.

Although 8 additional data bits, D_8-D_{15}, are available, the features most often used are the additional interrupt request and DMA request signals.

16-Bit ISA BUS

Back of computer





16-bit connector

1	MCS16	BHE
2	IOCS16	A23
3	IRQ10	A22
4	IRQ11	A21
5	IRQ12	A20
6	IRQ15	A19
7	IRQ14	A18
8	DACK0	A17
9	DRQ0	MEMR
10	DACK5	MEMW
11	DRQ5	D8
12	DACK6	D9
13	DRQ6	D10
14	DACK7	D11
15	DRQ7	D12
16	+5V	D13
17	MASTER	D14
18	GND	D15

Source: http://smallformfactors.mil-embedded.com/articles/isa-bus-going-strong-pc104/

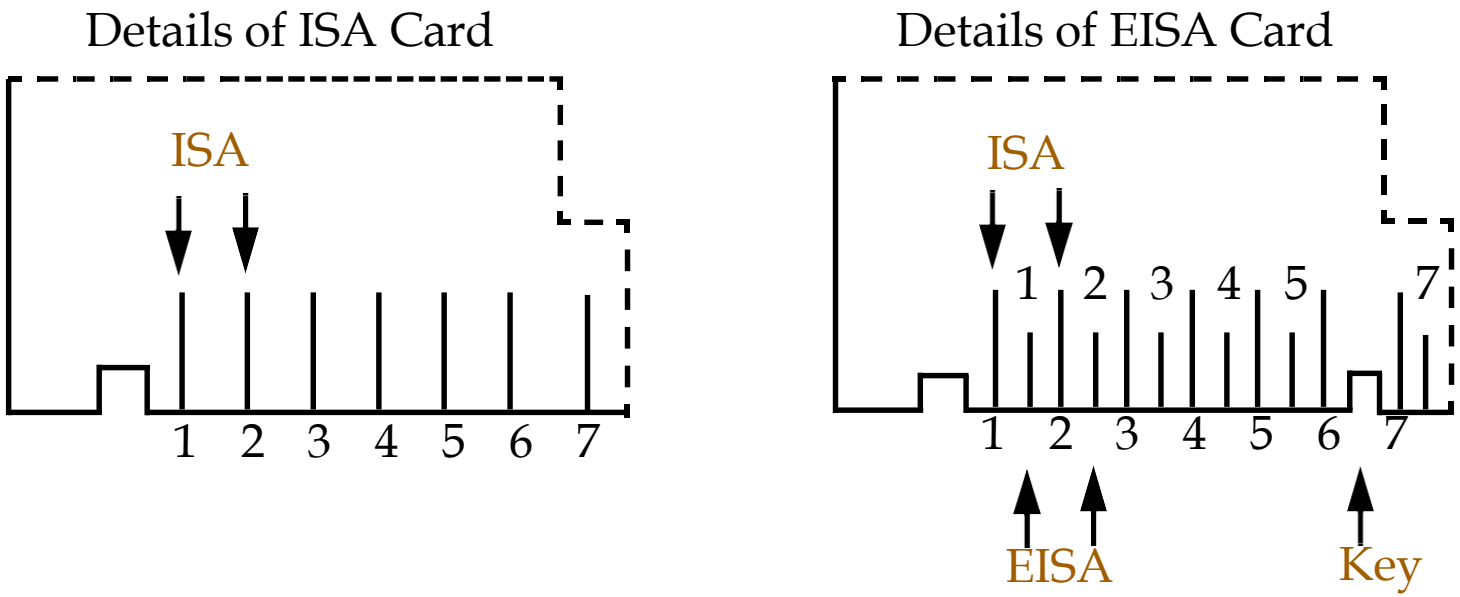
EISA Bus

Extended ISA (EISA) has a 32-bit data bus but still operates at 8MHz.

It is rarely used -- mainly as a disk controller or video graphics adapter.

New pins for EISA bus are interspersed with the older pins in the 16-bit ISA connector to preserve compatibility with the old standard.

Most of the new EISA connections are used for the 32-bit data and 32-bit latched address bus.



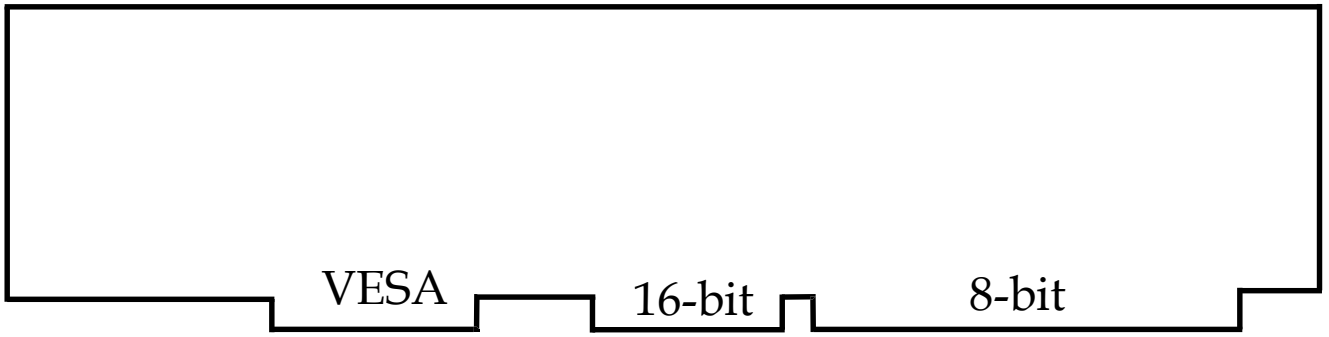
VESA Local Bus

VESA (VL bus) is a 33MHz extension of the ISA bus used of high-speed data transfer applications.

It contains 32-bit address and data bus and is mainly used for video and disk interfaces.

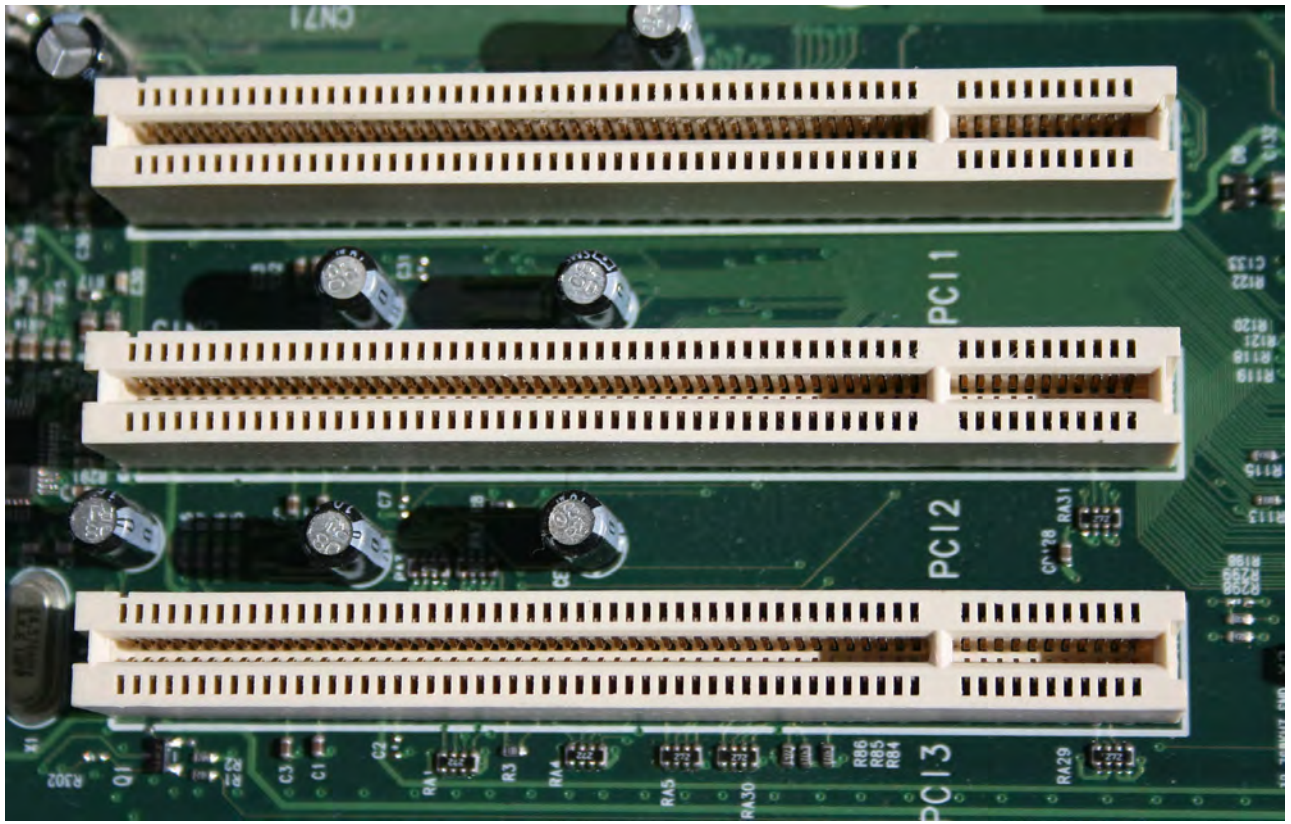
Requires a third connector (VESA connector) to be added behind the standard 16-bit ISA connector.

VESA local Bus Card



Peripheral Component Interconnect (PCI) Bus

PCI became common due to plug-and-play characteristics and ability to function with 64-bit data bus.



Source: Wikimedia Commons

Peripheral Component Interconnect (PCI) Bus

A PCI interface contains a series of registers, located in a small memory device, that contain information about the board.

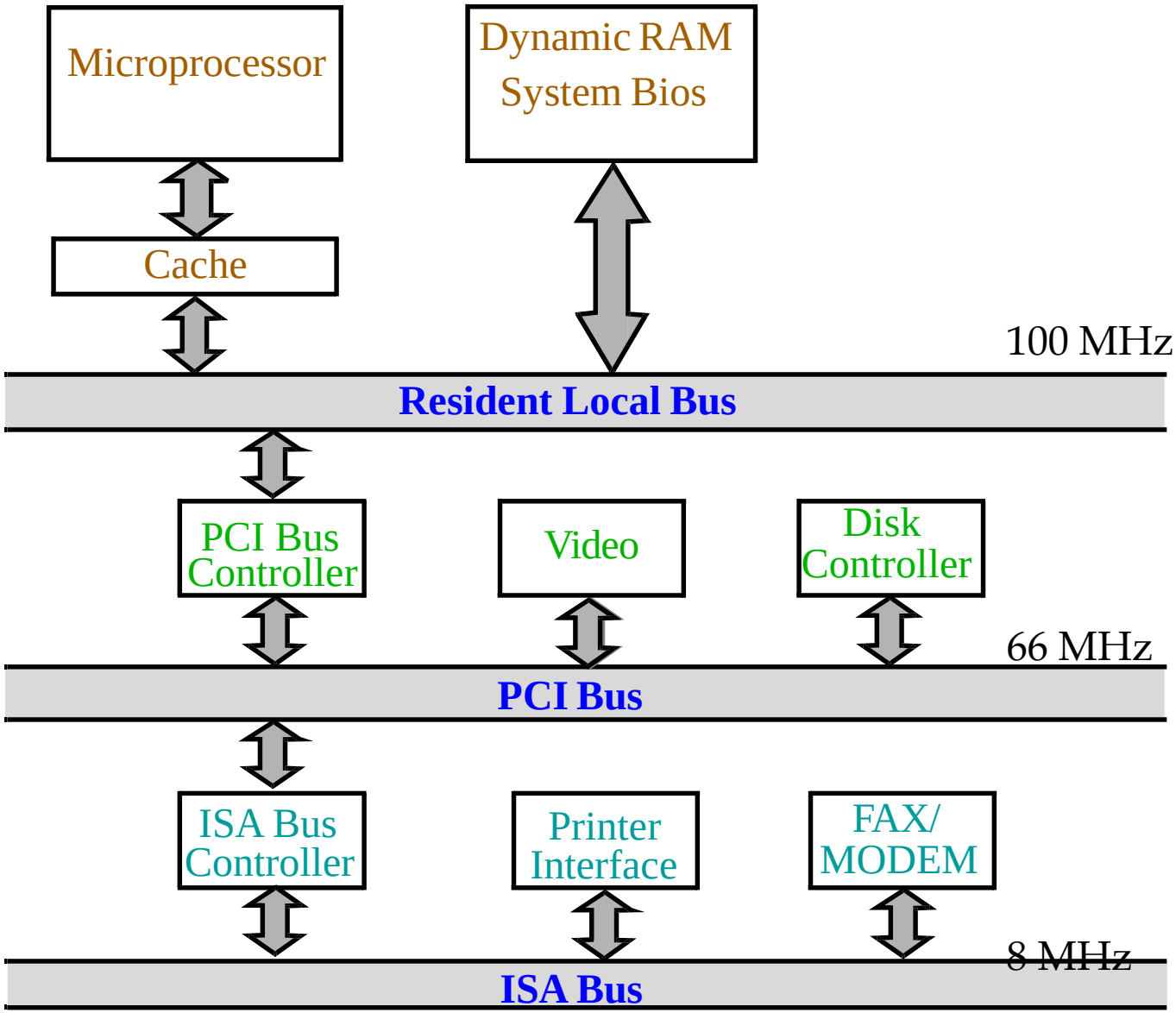
The information in this registers allow the computer to automatically configure the PCI card (Plug-and-Play ***PnP*** feature).

The microprocessor connects to the PCI bus through an integrated circuit called a **PCI Bridge** thus making the PCI bus independent of processor type and architecture.

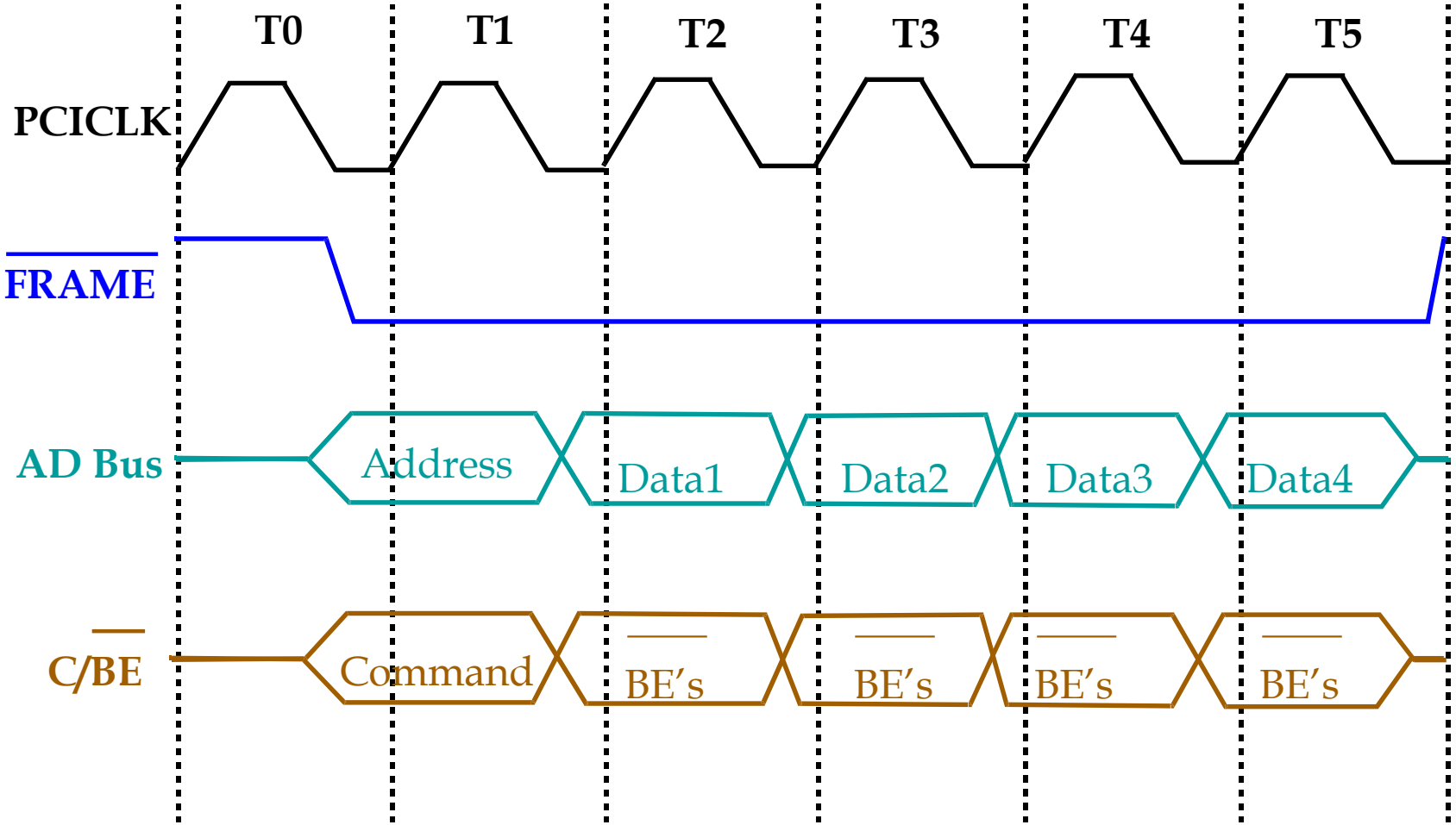
PCI functions with either a 32-bit or 64-bit address and data bus.

- The address and data buses are multiplexed to reduce the size of the edge connector.
- 32-bit and 64-bit cards.
- Newest versions run at 66 MHz (twice the older 33 MHz version).

PCI Bus System Structure



PCI Timing Diagram

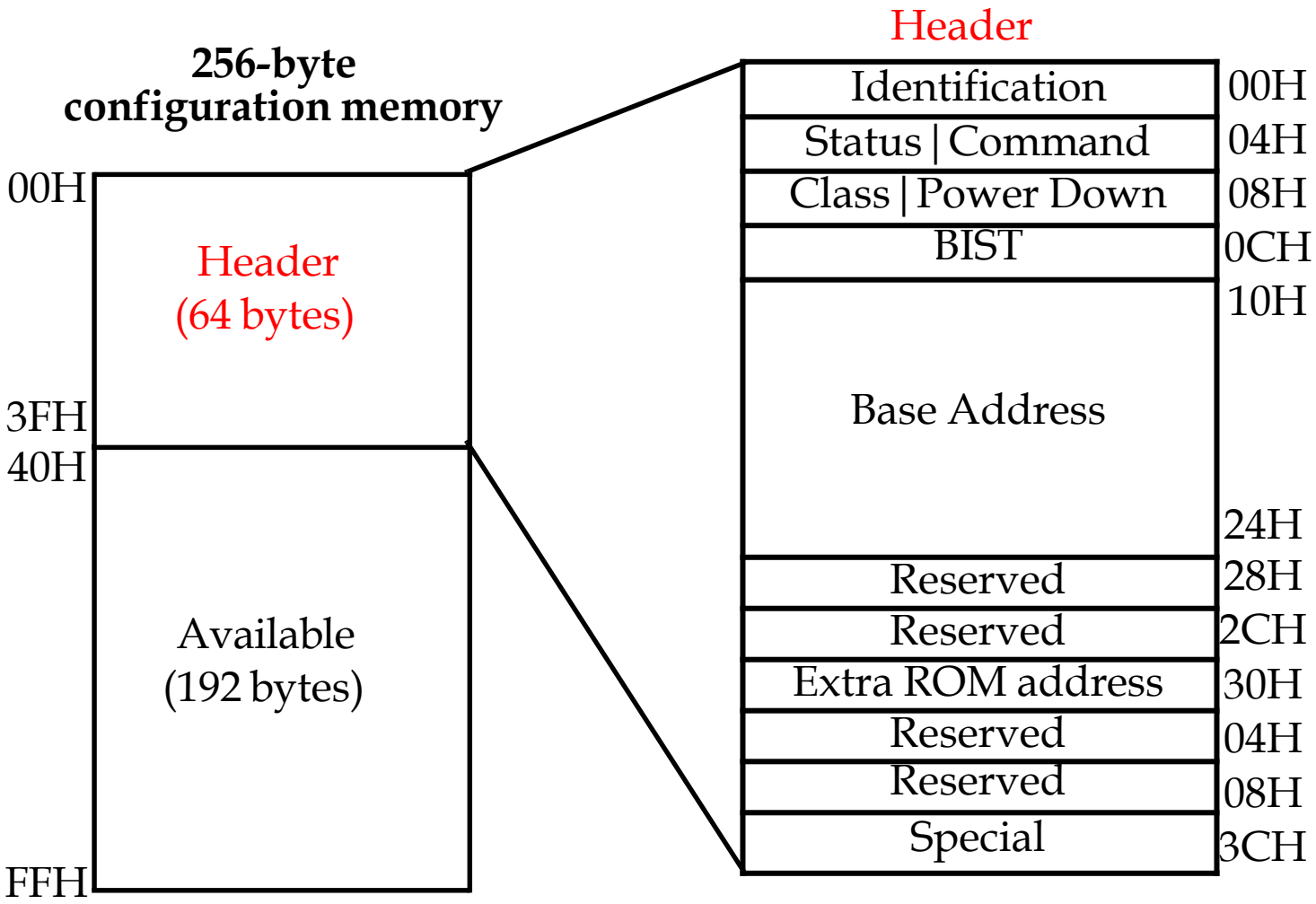


PCI Bus Commands

The following commands can appear on the C/$\overline{\text{BE}}$ pins in cycle T1.

- I**NTA Sequence**: Get the interrupt vector from the interrupt controller. The interrupt vector byte is returned during a read operation.
- **Special Cycle**: Used to transfer data to all PCI components, e.g. processor shutdown.
- **I/O Read Cycle:** Data are read from an I/O device at address AD0-AD15.
- **I/O Write Cycle:** Data are written to an I/O device.
- **Memory Read Cycle**: Data are read from memory device.
- **Memory Write Cycle:** Data are written to memory device.
- **Configuration Read:** Configuration information is read from PCI device
- **Configuration Write:** Configuration information is written to PCI device.
- **Memory Multiple Access:** Multiple data are read from memory device.
- **Dual Addressing Cycle:** Used for transferring data to a 64-bit PCI device which only contains a 32-bit data path.
- **Line Memory Access:** Used to read more than two 32-bit numbers.
- **Memory Write with Invalidation:** Same as line memory access, but used with write and bypasses write-back function of the cache.

PCI Bus Configuration Space



PCI Bus Configuration Space

The PCI interface contains 256-byte configuration memory that allows plug-and-play feature.

The header holds information about the PCI interface.

The header contains the *unit ID*, *vendor ID*, *class code* and manufacturer defined bits. The vendor ID and class ID are allocated by PCI SIG.

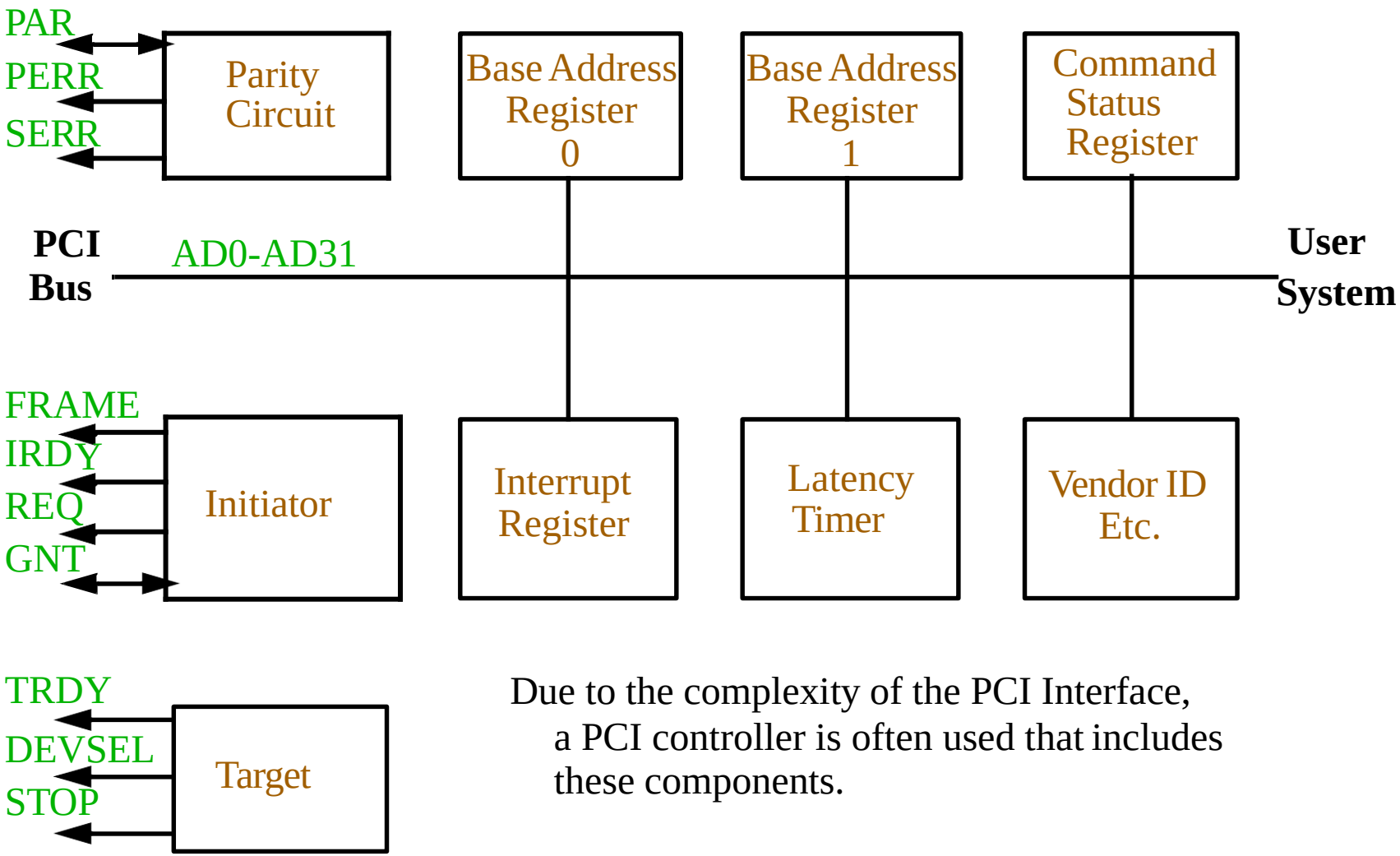
The base address space consists of a base address for the memory, a second for the I/O space and the third for the expansion ROM.

When a PCI bus is present, the system BIOS is extended to support it.

Access to this extended BIOS is through interrupt vector 1AH. (See text for the currently available functions.)

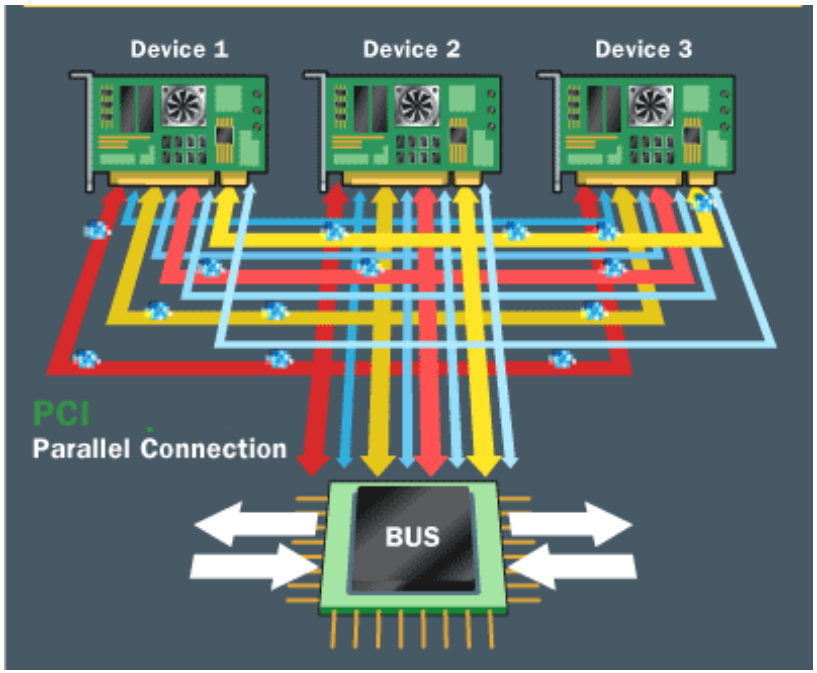
Once the presence of the BIOS is established, the contents of the configuration memory can be read using other BIOS functions.

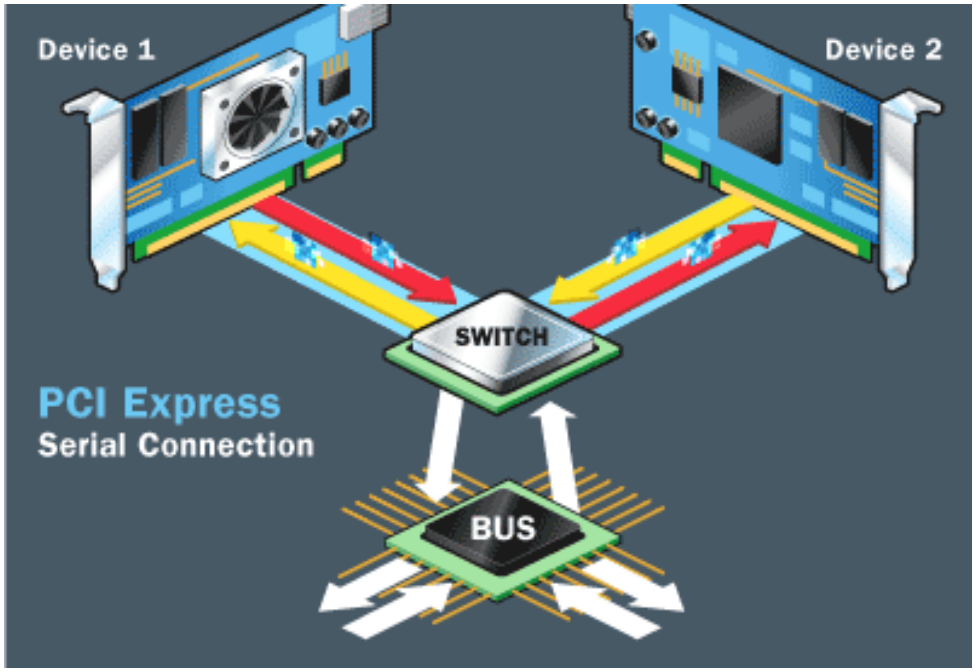
PCI Interface Block Diagram



Due to the complexity of the PCI Interface, a PCI controller is often used that includes these components.

PCI Express





Source: https://computer.howstuffworks.com/pci-express2.htm

PCI Express

Year	Bandwidth	Frequency/Speed
1992	133MB/s (32 bit simplex)	33 Mhz (PCI)
1993	533MB/s (64 bit simplex)	66 Mhz (PCI 2.0)
1999	1.06GB/s (64 bit simplex)	133 Mhz (PCI-X)
2002	2.13GB/s (64 bit simplex)	266 Mhz (PCI-X 2.0)
2002	8GB/s (x16 duplex)	2.5 GHz (PCIe 1.x)
2006	16GB/s (x16 duplex)	5.0 GHz (PCIe 2.x)
2010	32GB/s (x16 duplex)	8.0 GHz (PCIe 3.x)
2017	64GB/s (x16 duplex)	16.0 GHz (PCIe 4.0)
2019	128GB/s (x16 duplex)	32.0 GHz (PCIe 5.0)

Source: https://www.nextplatform.com/2017/07/14/system-bottleneck-shifts-pci-express/

The Universal Serial Bus (USB)

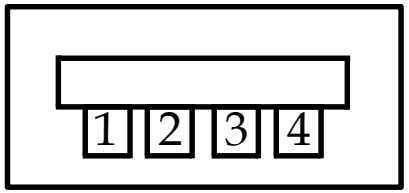
Allows access of up to 127 different connections via a 4 wire serial connection.

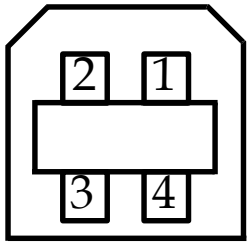
This interface is ideal for keyboards, sound cards, modems, etc.

Sound cards can derive their power from an external (no-PC) power supply.

Cable lengths are limited to 5 meters (for the full-speed interface).

Maximum power is given by 100mA x 5V.



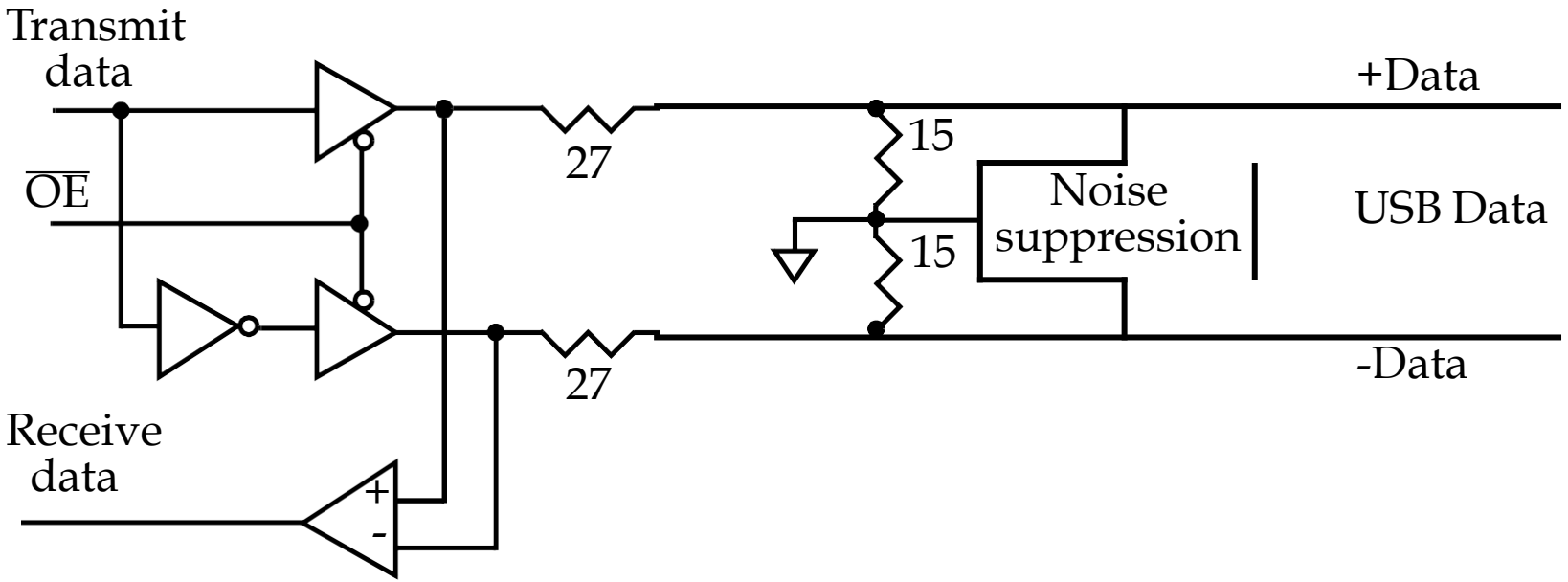


Pin #	Signal
1	5.0 V
2	-Data
3	+Data
4	GND

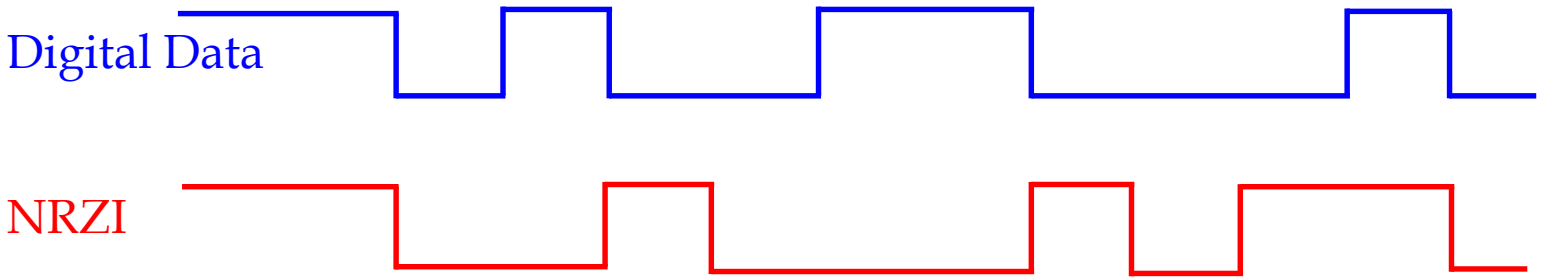
The +/-Data signals are 180 degrees out of phase.

The Universal Serial Bus (USB)

The following circuit can be used to generate the biphase signals.

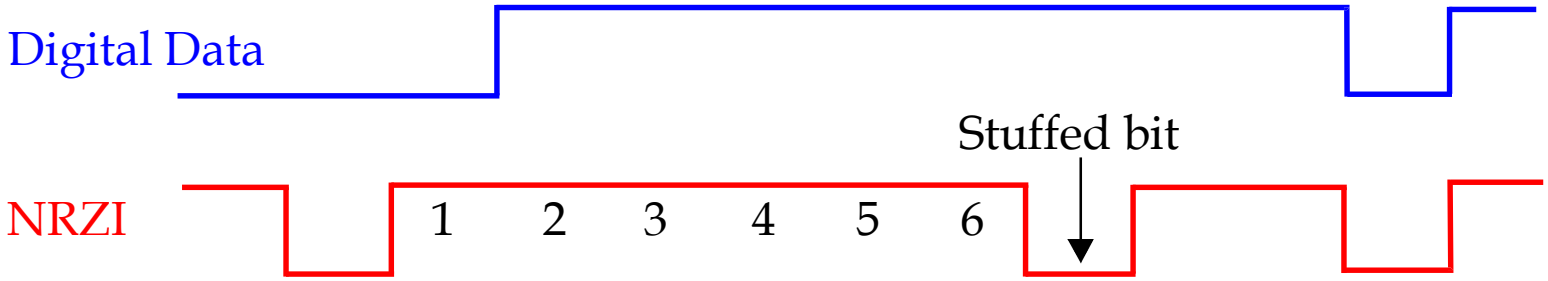


Data packets are sent and received using a NRZI (non-return to zero, inverted) data encoding.



The Universal Serial Bus (USB)

Since the transmitter and receiver must remain synchronized and a large string of 1's do not generate any pulses, a bit may be 'stuffed'.



Here, a bit is added to force a change in the signal line.

USB Commands:

Communication begins with a *sync byte* (80H), followed by a packet identification byte (PID).

The PID contains 8 bits -- the rightmost four bits contain the type of packet that follows (if any).

The leftmost 4 bits are the compliment (used for error detection.)

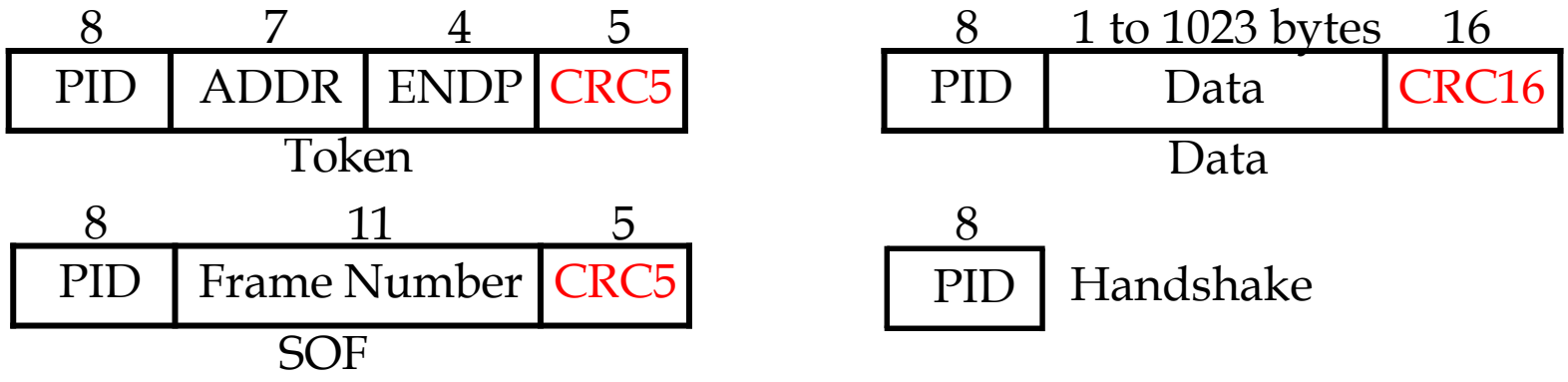
For example, if command is 1000 and 0111 1000 is sent.

The Universal Serial Bus (USB)

PIDs are available for token indicators, data indicators and handshaking:

PID	Name	Type	Description
E1H	OUT	Token	Host->function transaction
D2H	ACK	Handshake	Receiver accepts packet
C3H	Data0	Data	Data packet PID even
A5H	SOF	Token	Start of Frame
69H	IN	Token	Function -> host transaction
5AH	NAK	Handshake	Receiver does not accept data
4BH	Data1	Data	Data packet PID odd
3CH	PRE	Special	Host preamble
2DH	Setup	Token	Setup command
1EH	Stall	Token	Stalled

Formats of the data, token, handshaking and start-of-frame are as follows:



The Universal Serial Bus (USB)

Two types of CRC (cyclic redundancy check):

- 5-bit CRC for tokens, SOF, etc.

  Primitive polynomial is $X^5 + X^2 + 1$

- 16-bit CRC for data.

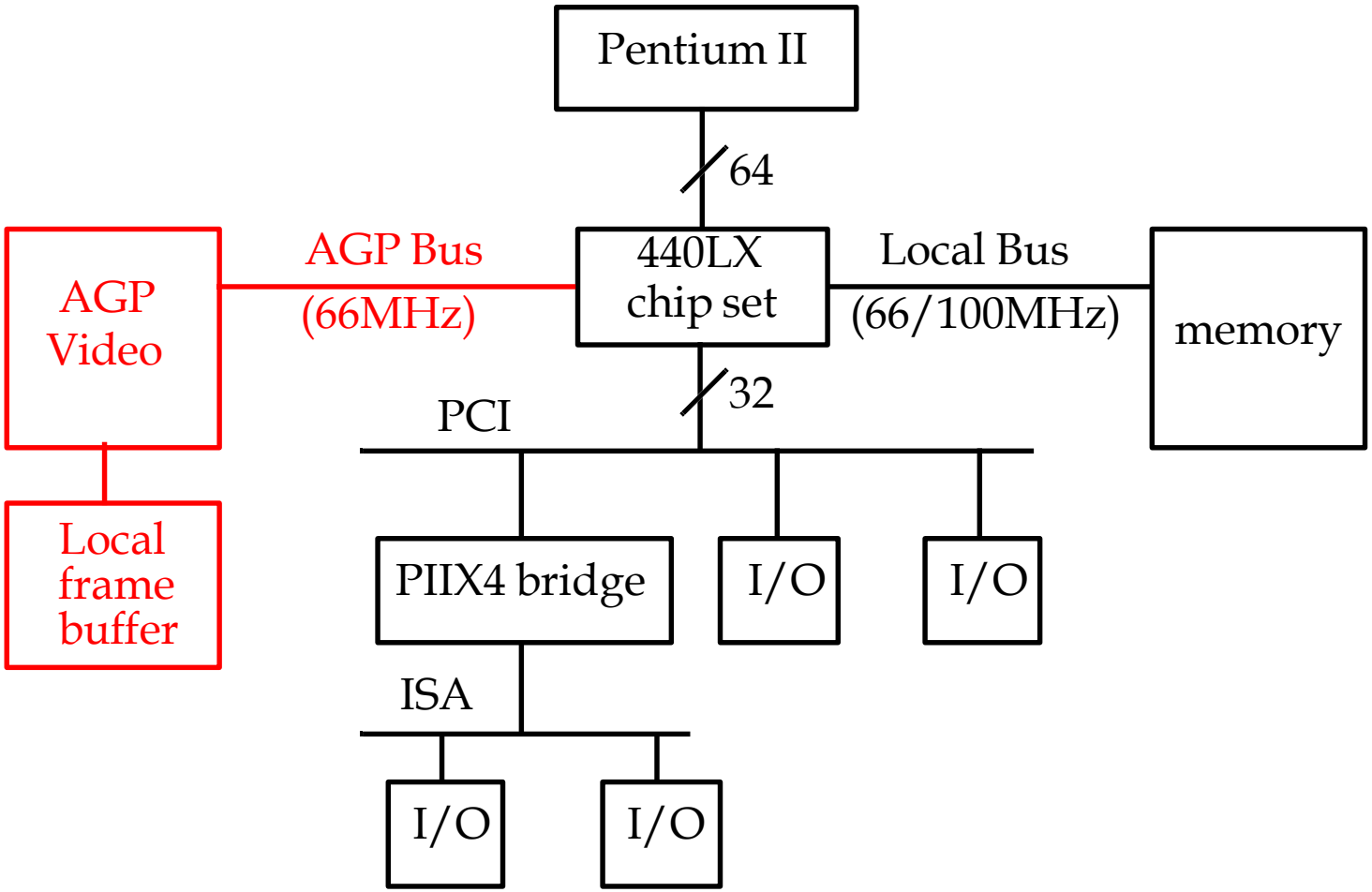
  Primitive polynomial is $X^{16} + X^{15} + X^2 + 1$

The handshaking PID packets are used to signal errors between the transmitter and receiver.

A NAK causes the transmitter to resend the data.

This is called **stop and wait flow control** since the transmitter must wait for an ACK before sending any additional packets.

AGP Graphics Port



Operates at system bus speed, e.g. 528M bytes/sec under the 2X compliant system and over 1 G bytes/sec under a 4X.

PCI maximum is ~100 M bytes/sec.