UMBC

CMPE-310

Lecture-06: Memory I

Outline

Memory Chips

ROM

EPROM

SRAM

DRAM

Memory Chips

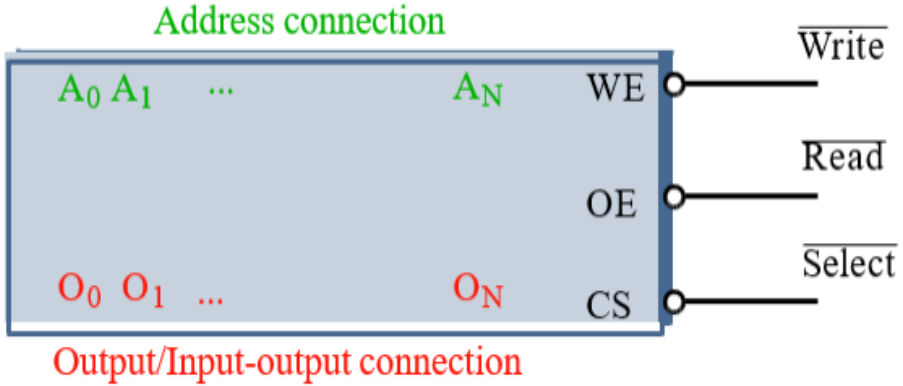
Memory Types

Two basic types:

ROM: Read-only memory

RAM: Read-Write memory

Generic pin configuration:



Four commonly used memories:

- **ROM**
- **Flash, EEPROM**
- **Static RAM (SRAM)**
- **Dynamic RAM (DRAM), SDRAM, RAMBUS, DDR**

Memory Chips

Address Pins

The number of **address pins** is related to the number of **memory locations**.

Common sizes today are **1K** to **256M** locations.

Therefore, between **10 and 28 address pins** are present.

Data Pins

The **data pins** are typically **bi-directional** in read-write memories.

The number of data pins is related to the **size of the memory location**.

For example, an 8-bit wide (byte-wide) memory device has **8** data pins.

Catalog listing of **1K X 8** indicate a byte addressable 8K bit memory with 10 address pins.

Memory Chips

Control Pins

Each memory device has at least one **chip select** (CS) or **chip enable** (CE) or **select** (S) pin that enables the memory device.

This enables read and/or write operations.

If more than one are present, then all must be **0** in order to perform a read or write.

Each memory device has at least one control pin.

For ROMs, an **output enable** (OE) or **gate** (G) is present.

The OE pin enables and disables a set of tristate buffers.

For RAMs, a **read-write** (R/W) or **write enable** (WE) and **read enable** (OE) are present.

For dual control pin devices, it must hold true that both are not **0** at the same time.

Memory Chips

ROM: Non-volatile memory: Maintains its state when powered down.

There are several forms:

ROM: Factory programmed, cannot be changed. Older style.

PROM: Programmable Read-Only Memory. Field programmable but only once. Older style.

EPROM: Erasable Programmable Read-Only Memory.

Reprogramming requires up to 20 minutes of high-intensity UV light exposure.

Flash, EEPROM: Electrically Erasable Programmable ROM.

Also called **EAROM** (Electrically Alterable ROM) and **NOVRAM** (NOn-Volatile RAM).

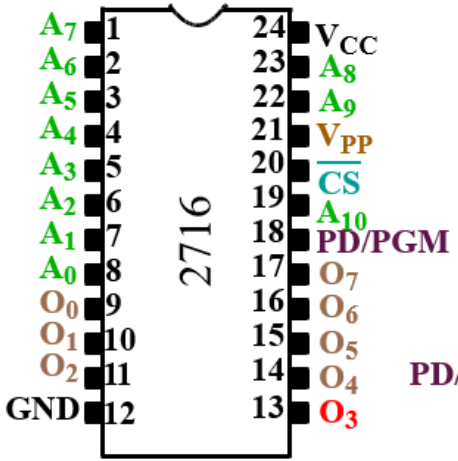
Writing is much slower than a normal RAM.

Used to store setup information, e.g. video card, on computer systems.

Can be used to replace EPROM for BIOS memory.

EPROMS

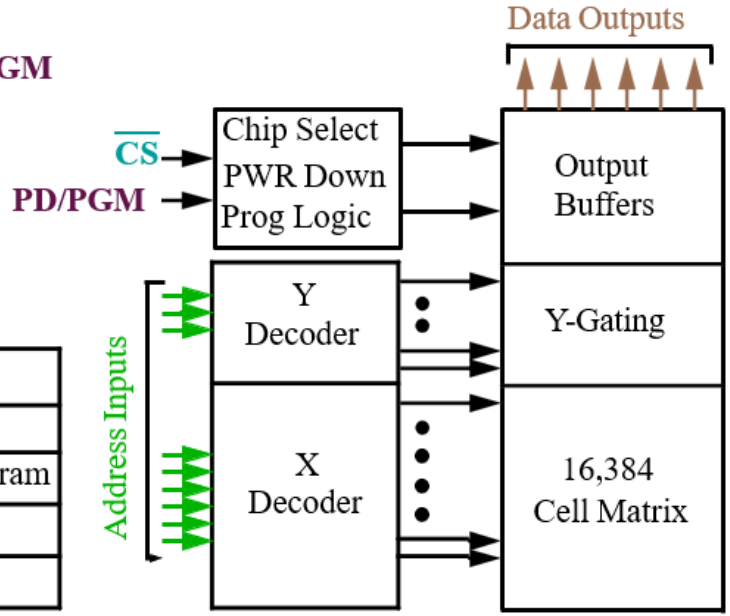
Intel 2716 EPROM (2K X 8):



2K x 8 EPROM

V_{PP} is used to program the device by applying 25V and pulsing PGM while holding $\overline{CS}$ high.

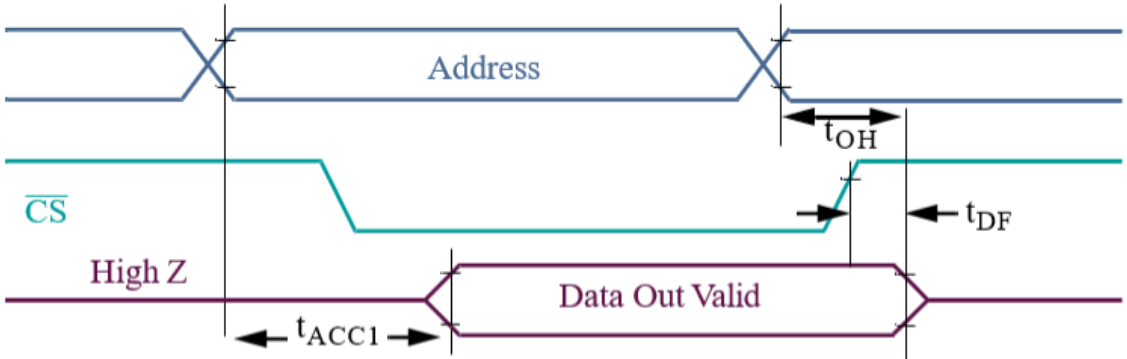
Pin(s)	Function
A_0-A_{10}	Address
PD/PGM	Power down/Program
$\overline{CS}$	Chip Select
O_0-O_7	Outputs



Adapted from lecture notes by Dr Chintan Patel and Avani Dave

EPROMS

2716 Timing diagram:



Read Mode (PD/PGM =V_{IL})

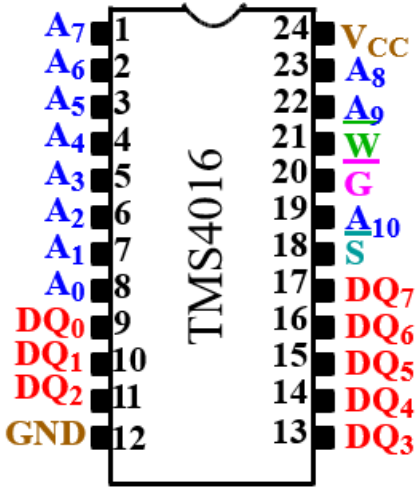
Sample of the data sheet for the 2716 A.C. Characteristics.

Symbol	Parameter	Limits			Unit	Test Condition
		Min	Typ.	Max		
t_{ACC1}	Addr. to Output Delay		250	450	ns	PD/PGM= CS =V_{IL}
t_{OH}	Addr. to Output Hold	0			ns	PD/PGM= CS =V_{IL}
t_{DF}	Chip Deselect to Output Float	0		100	ns	PD/PGM=V_{IL}
...	...	...	...	...	...	...

This EPROM requires a wait state for use with the 8086 (*460ns* constraint).

SRAMS

TI TMS 4016 SRAM (2K X 8):



2K x 8 SRAM

Pin(s)	Function
A_0-A_{10}	Address
DQ_0-DQ_7	Data In/Data Out
S (CS)	Chip Select
G (OE)	Read Enable
W (WE)	Write Enable

Virtually identical to the EPROM with respect to the pinout.

However, access time is faster (250ns).

See the timing diagrams and data sheets in text.

SRAMs used for *caches* have access times as low as *10ns*.

DRAMS

SRAMs are limited in size (up to about 128K X 8).
DRAMs are available in much larger sizes, e.g., 64M X 1.

DRAMs MUST be refreshed (rewritten) every 2 to 4 ms
Since **they store their value on an integrated capacitor that loses charge over time**.

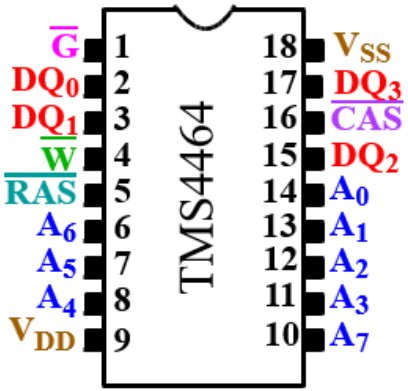
This refresh is **performed by a special circuit** in the DRAM which refreshes the entire memory.

Refresh also occurs on a normal read or write.

The large storage capacity of DRAMs make it impractical to add the required number of address pins. Instead, the address pins are multiplexed.

DRAMS

TI TMS4464 DRAM (64K X 4):



64K x 4 DRAM

Pin(s)	Function
A_0-A_7	Address
DQ_0-DQ_3	Data In/Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable

The TMS4464 can store a total of 256K bits of data.

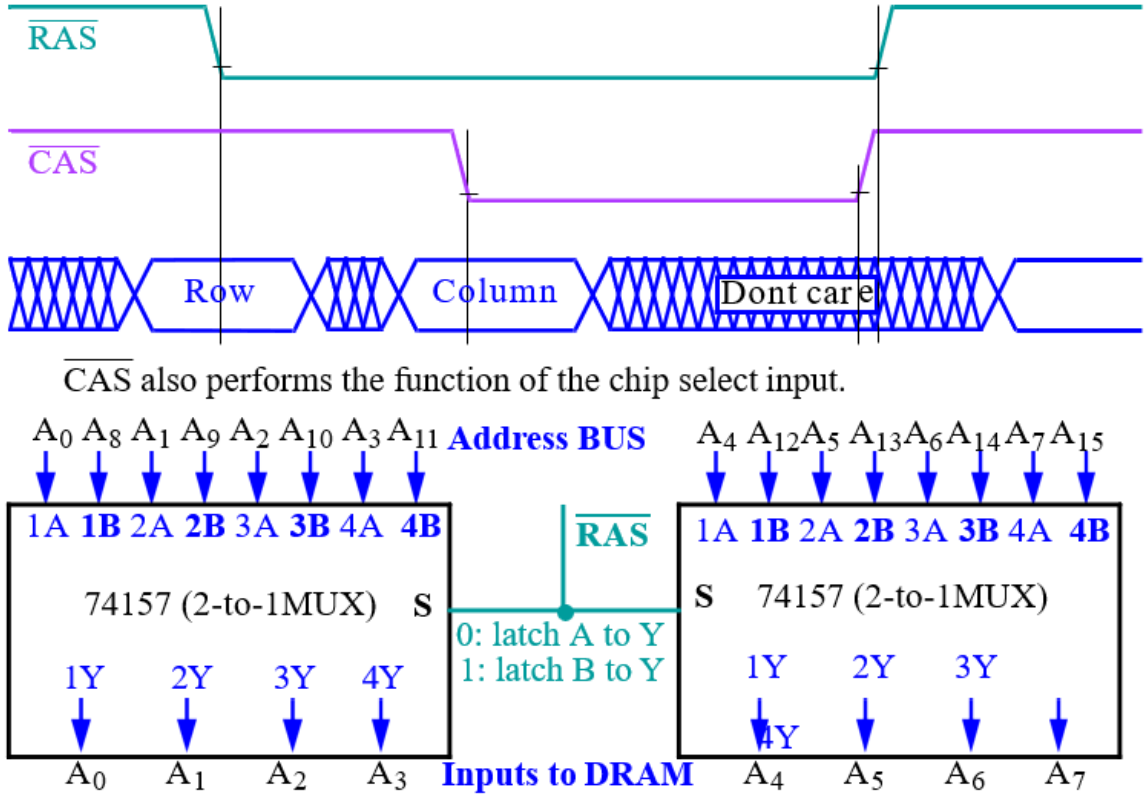
It has **64K** addressable locations which means it needs **16** address inputs, but it has only **8**.

The row address (A_0 through A_7) are placed on the address pins and strobed into a set of internal latches.

The column address (A_8 through A_{15}) is then strobed in using CAS.

DRAMS

TI TMS4464 DRAM (64K X 4) Timing Diagram:



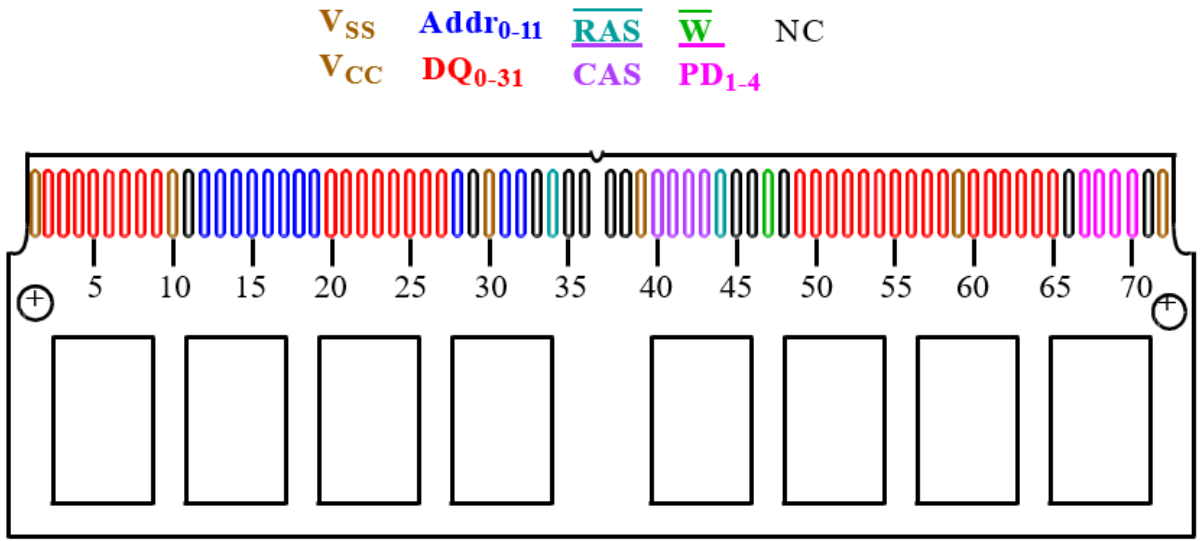
DRAMS

Larger DRAMs are available which are organized as *1M X 1*, *4M X 1*, *16M X 1*, *64M X 1*, *256M X 1*.

DRAMs are typically placed on SIMM **(Single In-line Memory Modules)** boards.

30-pin SIMMs come in *1M X 8*, *1M X 9* (parity), *4M X 8*, *4M X 9*.

72-pin SIMMs come in *1*/*2*/*3*/*8*/*16M X 32* or *1M X 36* (parity).



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DRAMS

Pentiums have a 64-bit wide data bus.

The **30-pin** and **72-pin** SIMMs are not used on these systems.

Rather, **64-bit DIMMs** (*Dual In-line Memory Modules)* are the standard.

These organize the memory 64-bits wide.

The board has DRAMs mounted on both sides and is **168** pins.

Sizes include *2M X 64* (**16M**), *4M X 64* (**32M**), *8M X 64* (**64M**) and *16M X 64* (**128M**).

The DIMM module is available in

DRAM, **EDO** and **SDRAM** (and **NVRAM**) with and without an EPROM.

The EPROM provides information about the size and speed of the memory device for **PnP** applications.

DRAMS

DDR SDRAM Standard	Internal rate (MHz)	Bus clock (MHz)	Prefetch	Data rate (MT/s)	Transfer rate (GB/s)	Voltage (V)
SDRAM	100-166	100-166	1n	100-166	0.8-1.3	3.3
DDR	133-200	133-200	2n	266-400	2.1-3.2	2.5/2.6
DDR2	133-200	266-400	4n	533-800	4.2-6.4	1.8
DDR3	133-200	533-800	8n	1066-1600	8.5-14.9	1.35/1.5
DDR4	133-200	1066-1600	8n	2133-3200	17-21.3	1.2

Image source: *Transcend Information Inc.*, transcend-info.com