UMBC

CMPE-310

Lecture-04: 8086 Chipset

Outline

8086 Device Specification

8086 Pinout

Clock Generator

Bus Timing (Read, Write)

MIN- MAX Mode

8086/88 Device Specifications

Both are packaged in DIP (Dual In-Line Packages)

- 8086: 16-bit microprocessor with a ***16-bit*** data bus
- 8088: 16-bit microprocessor with an ***8-bit*** data bus

Both are 5V parts (i.e. V_{DD} is 5V)

- 8086: Draws a maximum supply current of 360mA
- 8088: Draws a maximum supply current of 340mA

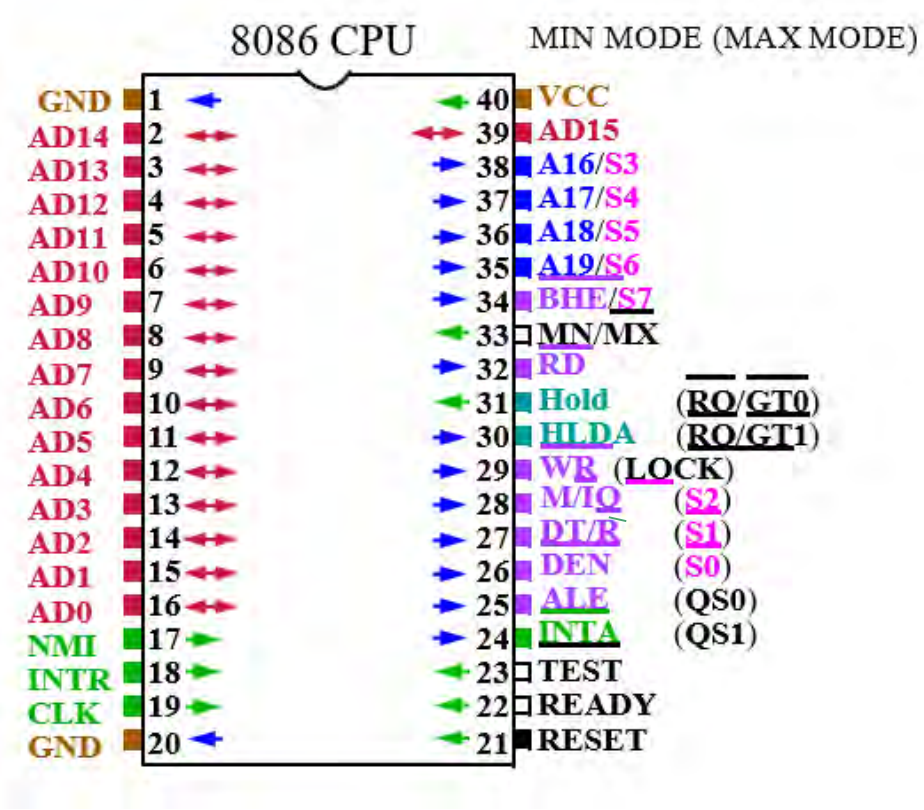
80C86/80C88: CMOS version draws 10mA with temp spec -40 to 225^{o}F

Input/Output current levels:

Input Logic level	Voltage	Current	Output Logic level	Voltage	Current
0	0.80V max	+/- 10uA max	0	0.45V max	+2mA max
1	2.0V min	+/- 10uA max	1	2.4 V min	-400uA max

Yields a 350mV noise immunity for logic 0 (Output max can be as high as 450mV while input max can be no higher than 800mV). This limits loading on the outputs.

8086 Pinout



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8086 Pinout

AD15-AD0

Multiplexed address(ALE=1)/data bus(ALE=0).

A19/S6-A16/S3 (multiplexed)

High order 4 bits of the 20-bit address OR status bits S6-S3.

$M/\overline{IO}$

Indicates if address is a Memory or IO address.

$\overline{RD}$

When 0, data bus is driven by memory or an I/O device.

$\overline{WR}$

Microprocessor is driving data bus to memory or an I/O device. When 0, data bus contains valid data.

ALE (Address latch enable)

When 1, address data bus contains a memory or I/O address.

$DT/\overline{R}$ (Data Transmit/Receive)

Data bus is transmitting/receiving data.

$\overline{DEN}$ (Data bus Enable)

Activates external data bus buffers.

8086 Pinout

S7, S6, S5, S4, S3, $\overline{S2}$, $\overline{S1}$, $\overline{S0}$

S7: Logic 1, **S6**: Logic 0.

S5: Indicates condition of IF flag bits.

S4-S3: Indicates which segment is accessed during current bus cycle

S4	S3	*Function*
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment

$\overline{S2}$, $\overline{S1}$, $\overline{S0}$: Indicate function of current bus cycle (decoded by 8288).

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	*Function*
0	0	0	Interrupt Ack
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	*Function*
1	0	0	Opcode Fetch
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	Passive

8086 Pinout

INTR

When 1 and IF=1, microprocessor prepares to service interrupt. $\overline{\textbf{INTA}}$ becomes active after current instruction completes.

$\overline{INTA}$

Interrupt Acknowledge generated by the microprocessor in response to INTR. Causes the interrupt vector to be put onto the address bus.

NMI

Non-maskable interrupt. Similar to INTR except IF flag bit is not consulted and interrupt is vector 2.

CLK

Clock input must have a duty cycle of 33% (high for 1/3 and low for 2/3s)

VCC/GND

Power supply (5V) and GND (0V)

MN/ $\overline{MX}$

Select minimum (5V) or maximum mode (0V) of operation.

8086 Pinout

$\overline{BHE}$

Bus High Enable. Enables the most significant data bus bits (D_{15}-D_8) during a read or write operation.

READY

Used to insert wait states (controlled by memory and IO for reads/writes) into the microprocessor.

RESET

Microprocessor resets if this pin is held high for 4 clock periods. Instruction execution begins at FFFF0H and IF flag is cleared.

$\overline{TEST}$

An input that is tested by the WAIT instruction. Commonly connected to the 8087 coprocessor.

HOLD

Requests a direct memory access (DMA). When 1, microprocessor stops and places address, data and control bus in high-impedance state.

HLDA (Hold Acknowledge)

Indicates that the microprocessor has entered the hold state.

8086 Pinout

$\overline{RO}/\overline{GT0}$ and $\overline{RO}/\overline{GT1}$ **:** Request/grant pins request/grant direct memory accesses (DMA) during maximum mode operation.

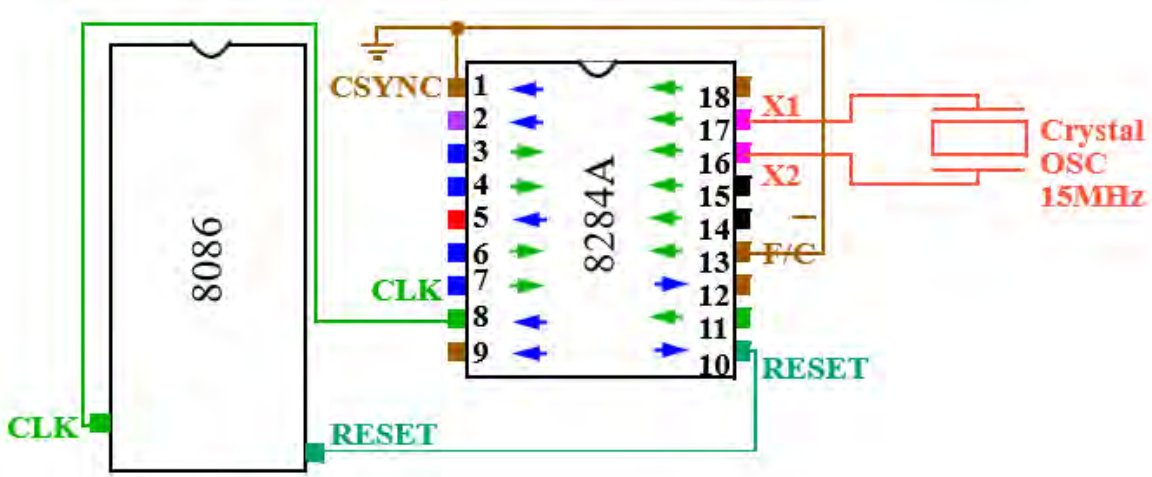
$\overline{LOCK}$ **:** Lock output is used to lock peripherals off the system. Activated by using the LOCK: prefix on any instruction.

QS1 and QS0 : The queue status bits show status of internal instruction queue. Provided for access by the numeric coprocessor (8087).

QS1	QS0	Status
0	0	No operation
0	1	First byte of op code from queue
1	0	Empty the queue
1	1	Subsequent byte from queue

8284A Clock Generator

- Clock generation
- RESET synchronization
- READY synchronization
- Peripheral clock signal



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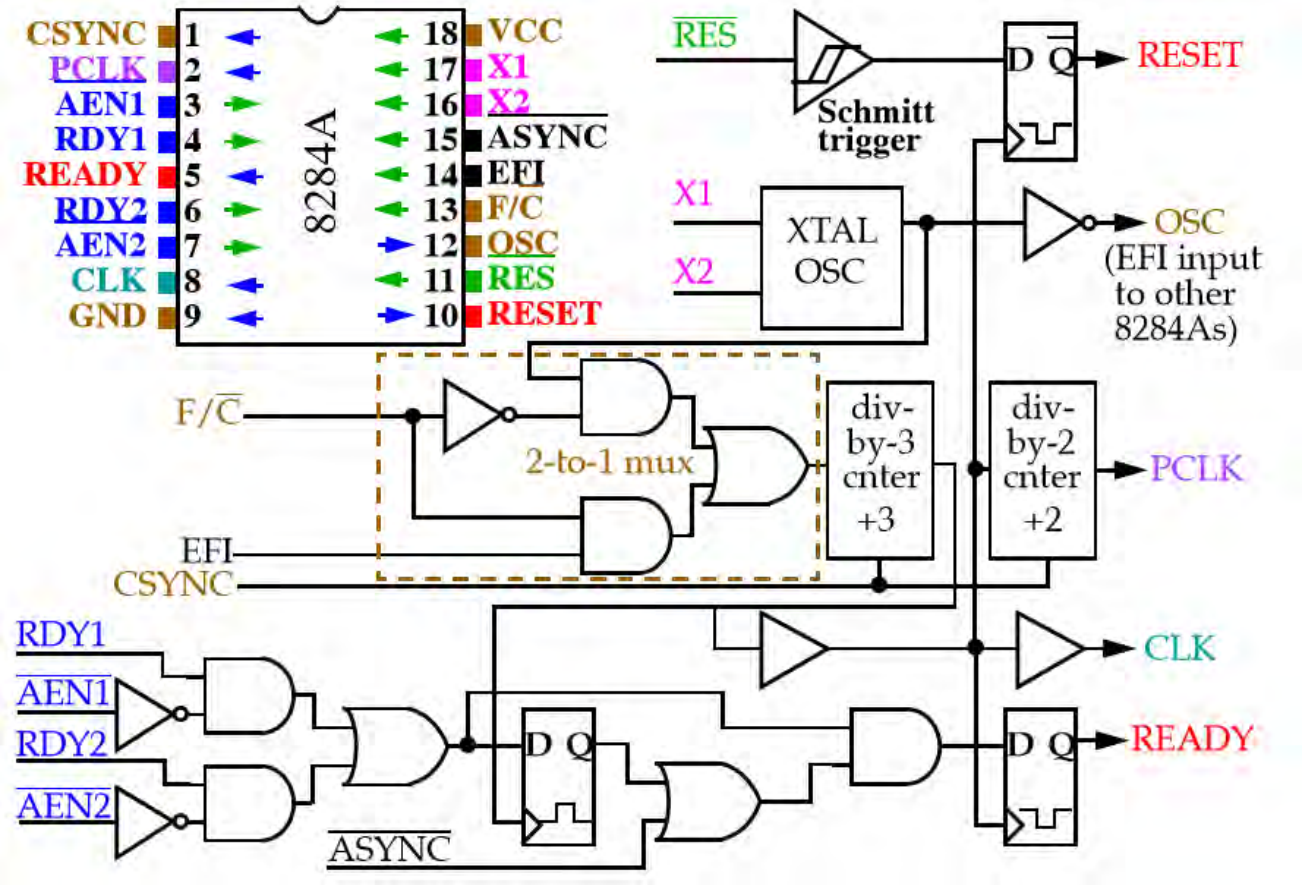
8284A Clock Generator



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8284A Clock Generator

Crystal is connected to X1 and X2.

XTAL OSC generates **square wave signal** at crystal's frequency which feeds:

An **inverting buffer** (output OSC) which is used to drive the EFI input of other 8284As.

2-to-1 MUX : F/C selects XTAL or EFI external input.

The MUX drives a divide-by-3 counter (**15 MHz to 5 MHz**).

This drives:

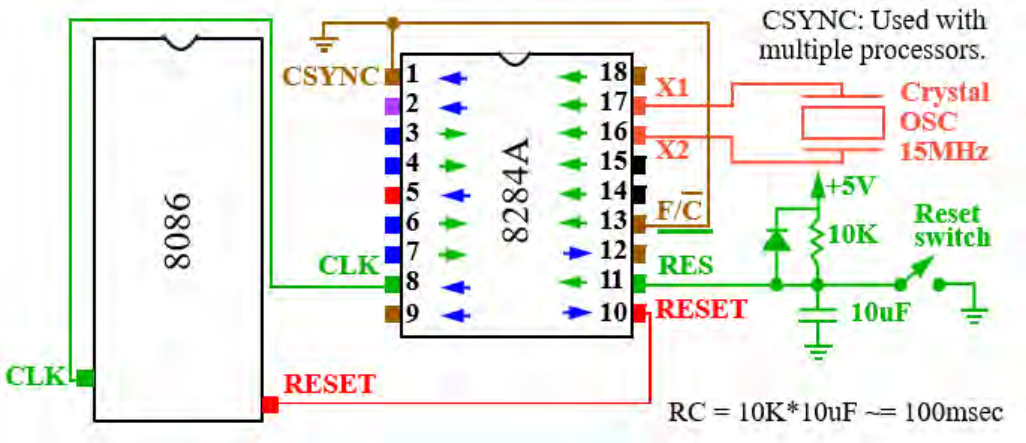
- The ***READY*** flip flop (READY synchronization).
- A second ***divide-by-2 counter*** (2.5MHz clk for peripheral components).
- The ***RESET*** flip flop.
- ***CLK*** which drives the 8086 CLK input.

8284A Clock Generator

RESET

Negative edge-triggered flip flop applies the RESET signal to the 8086 on the falling edge.

The 8086 samples the ***RESET*** pin on the rising edge.



Correct reset timing requires that the ***RESET*** input to the microprocessor becomes a logic 1 *NO LATER* than 4 clocks after power up and stay high for at least 50ms.

Bus buffering and latching

Computer systems have three buses

- Address
- Data
- Control

The Address and Data bus are ***multiplexed (shared)*** due to pin limitations on the 8086.

The ALE pin is used to control a set of latches.

All signals MUST be buffered Buffered Latches for A_0-A_{15}.

Control and A_{16}-A_{19} + $\overline{\boldsymbol{BHE}}$ are buffered separately. Data bus buffers must be bidirectional buffers.

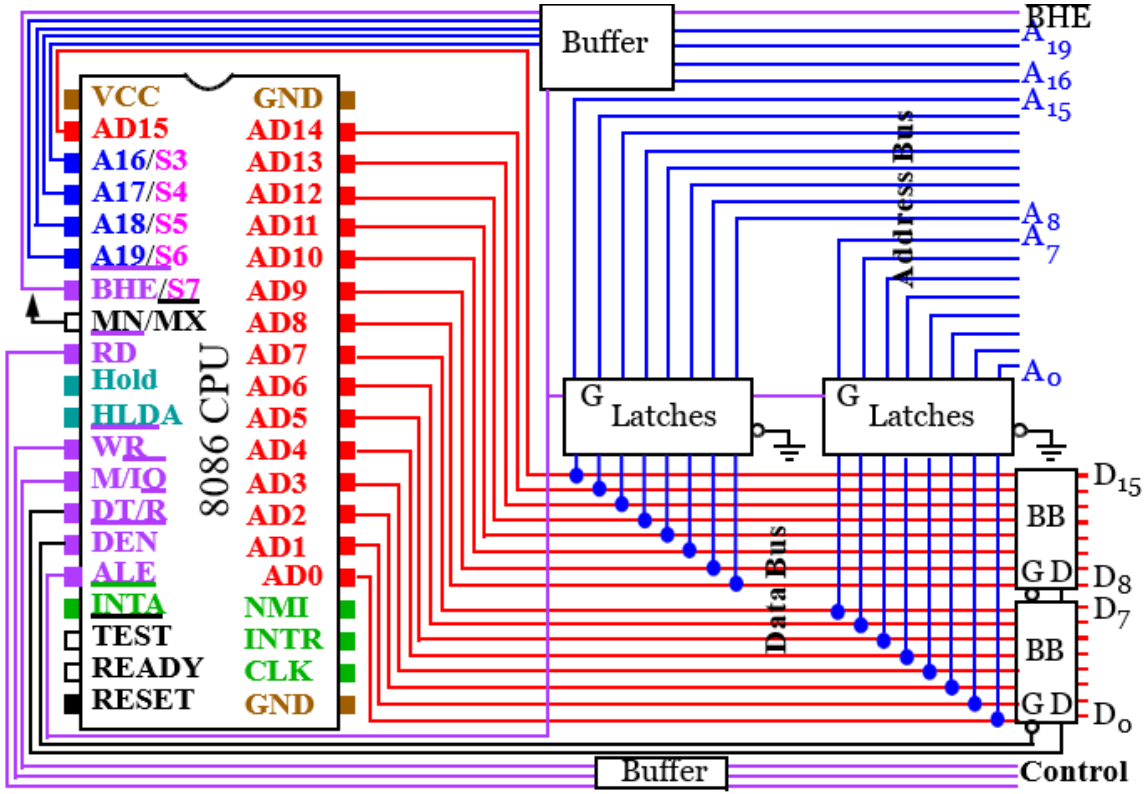
In a 8086 system, the memory is designed with two banks

High bank contains the higher order 8-bits and low bank the lower order 8-bits

Data can be transferred as 8 bits from either bank or 16-bits from both

$\overline{\boldsymbol{BHE}}$ pin selects the high-order memory bank

Bus buffering and latching



Adapted from lecture notes by Dr Chintan Patel and Avani Dave

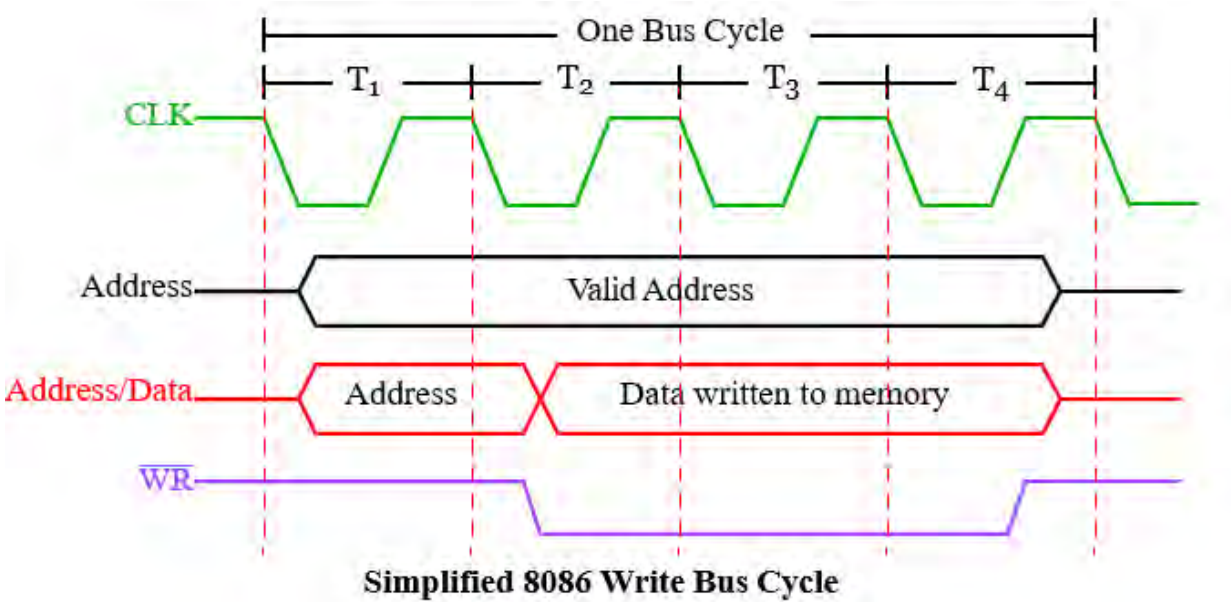
Bus Timing

Writing:

Dump address on address bus.

Dump data on data bus.

Issue a write ($\overline{WR}$) - set **M/$\overline{IO}$** to 1.

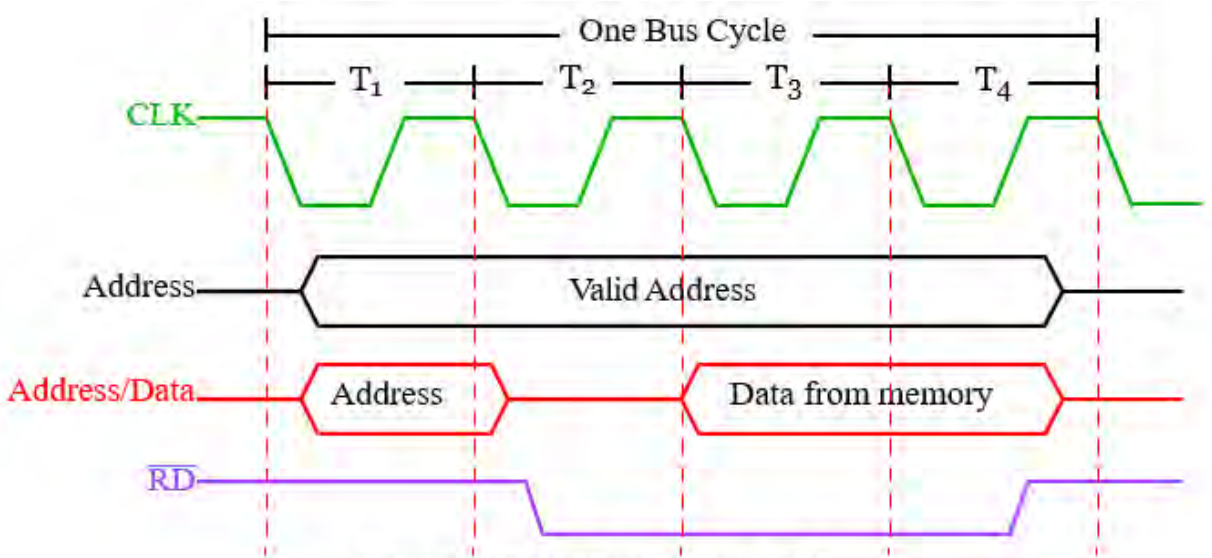


Simplified 8086 Write Bus Cycle

Bus Timing

Reading:

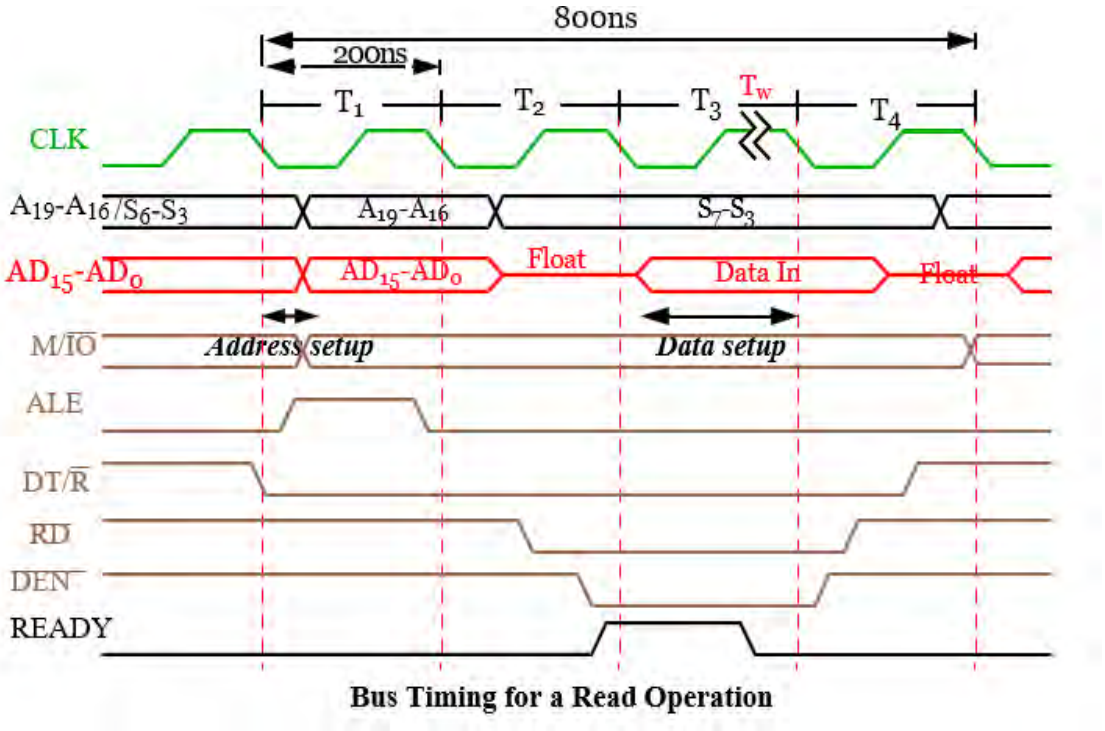
Dump address on address bus.
Issue a read ($\overline{RD}$) - set **M/$\overline{IO}$** to 1.
Wait for memory access cycle.



Simplified 8086 Read Bus Cycle

Bus Timing

Read Bus Timing:



Bus Timing for a Read Operation

Adapted from lecture notes by Dr Chintan Patel and Avani Dave

Bus Timing

During T_1:

The address is placed on the Address/Data bus.

Control signals M/IO, ALE and DT/R specify memory or I/O, latch the address onto the address bus and set the direction of data transfer on data bus.

During T_2:

8086 issues the RD or WR signal, DEN, and, for a write, the data.

DEN enables the memory or I/O device to receive the data for writes and the 8086 to receive the data for reads.

During T_3:

This cycle is provided to allow memory to access data.

READY is sampled at the end of T_2.

If low, T_3 becomes a wait state.

Otherwise, the data bus is sampled at the end of T_3.

During T_4:

All bus signals are deactivated, in preparation for next bus cycle.

Data is sampled for reads, writes occur for writes.

Bus Timing

Each **BUS CYCLE** on the 8086 equals ***four*** system clocking periods (T states).

The clock rate is ***5MHz***, therefore one Bus Cycle is ***800ns***.

The transfer rate is ***1.25MHz***.

Memory specifications (memory access time) must match constraints of system timing.

For example, bus timing for a read operation shows almost ***600ns*** are needed to read data.

However, memory must access faster due to setup times, e.g. Address setup and data setup.

This subtracts off about ***150ns***.

Therefore, memory must access in at least ***450ns*** minus another ***30-40ns*** guard band for buffers and decoders.

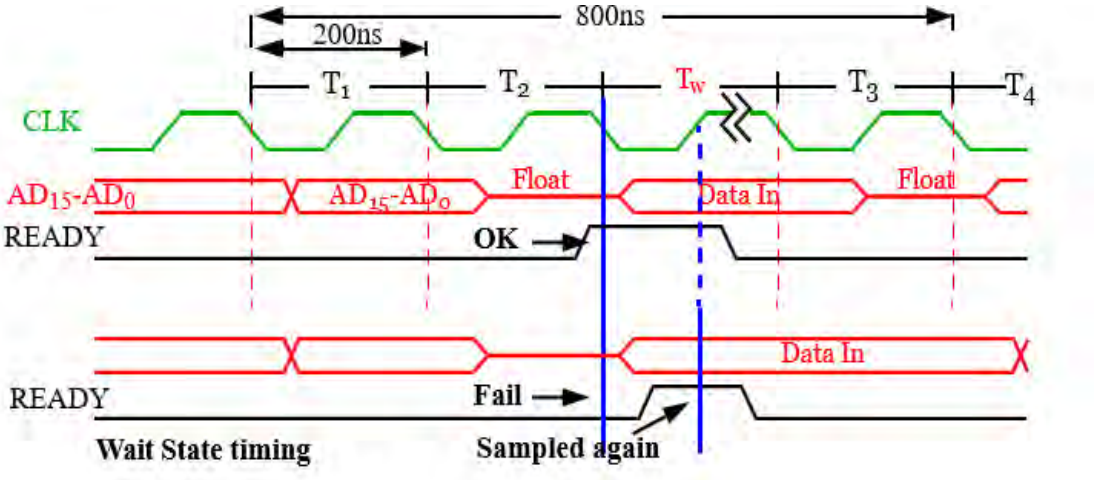
420ns DRAM required for the 8086.

Bus Timing

READY

An input to the 8086 that causes wait states for slower memory and I/O components. **A wait state (T_W) is an extra clock period inserted between T_2 and T_3 to lengthen the bus cycle**.

For example, this extends a ***460ns*** bus cycle (at 5MHz clock) to ***660ns***.



MIN and MAX mode

Controlled through the ***MN/$\overline{MX}$*** pin.

- ***Minimum mode*** is cheaper since all control signals for memory and I/O are generated by the microprocessor.
- ***Maximum mode*** is designed to be used when a coprocessor (8087) exists in the system.

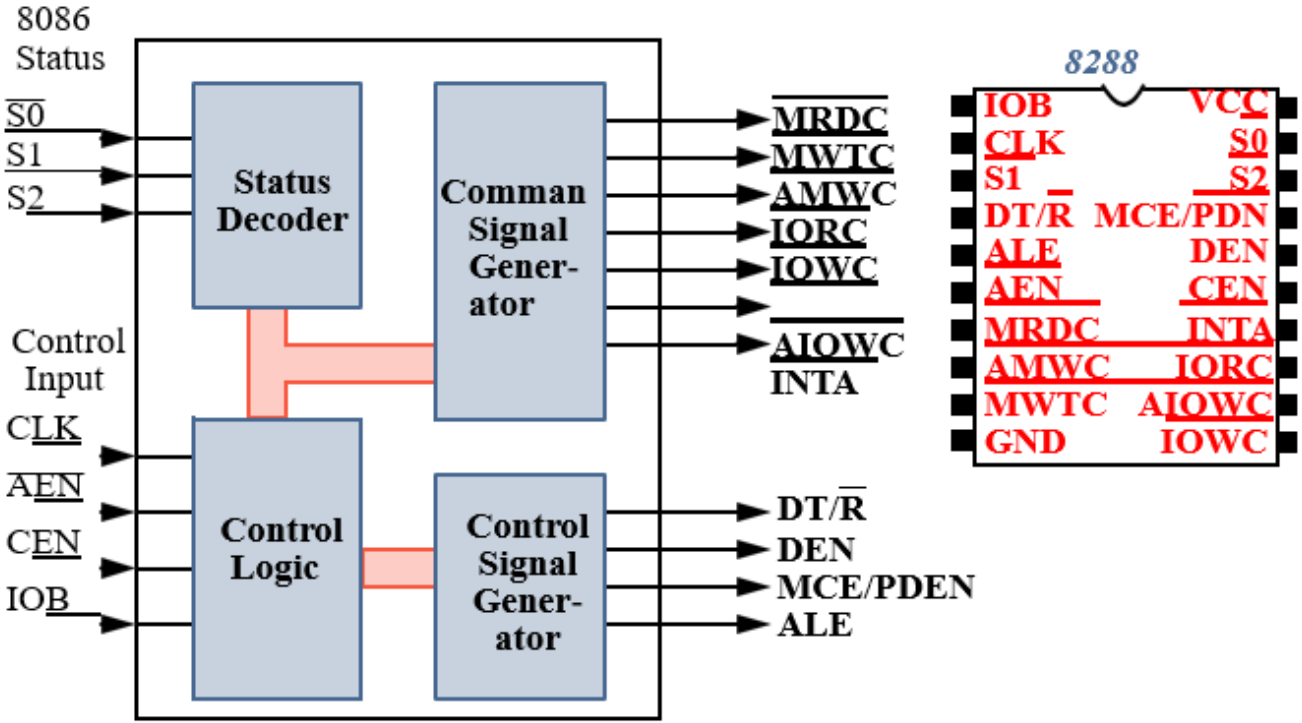
Some of the control signals must be generated externally, due to redefinition of certain control pins on the 8086.

The following pins are lost when the 8086 operates in ***Maximum mode***.

- ALE
- $\overline{WR}$
- IO/$\overline{M}$
- DT/$\overline{R}$
- $\overline{DEN}$
- $\overline{INTA}$

This requires an external bus controller: ***8288 Bus Controller***.

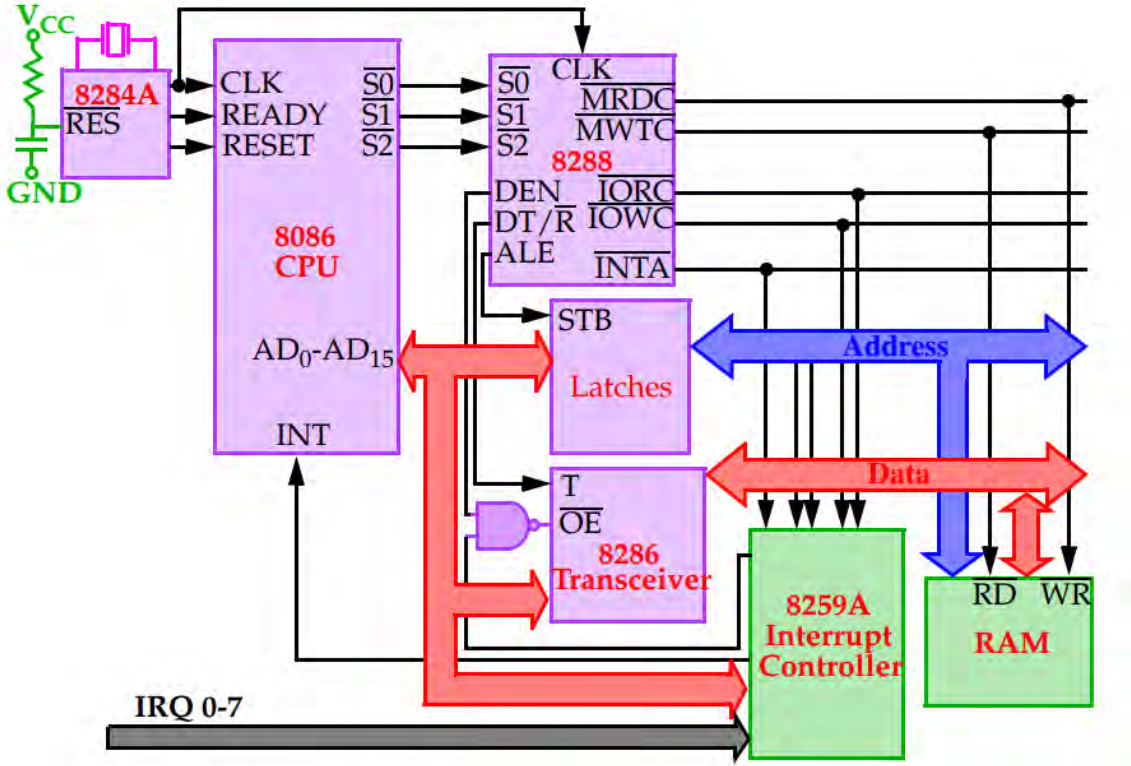
8288 Bus controller



Separate signals are used for I/O ($\overline{\text{IORC}}$ and $\overline{\text{IOWC}}$) and memory ($\overline{\text{MRDC}}$ and $\overline{\text{MWTC}}$).

Also provided are advanced memory ($\overline{\text{AIOWC}}$) and I/O ($\overline{\text{AIOWC}}$) write strobes plus $\overline{\text{INTA}}$.

Max Mode 8086 system



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